High performance organic electrochemical transistors and logic circuits manufactured via a combination of screen and aerosol jet printing techniques

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Keywords: aerosol jet printing, screen printing, OECT, PEDOT:PSS, printed electronics

Abstract

This work demonstrates a novel fabrication approach based on the combination of screen and aerosol jet printing to manufacture fully printed organic electrochemical transistors (OECT) and OECT-based logic circuits on PET substrates with superior performances. The use of aerosol jet printing allows for a reduction of the channel width to ~15 μm and the estimated volume by a factor of ~40, compared to the fully screen printed OECTs. Hence, the OECT devices and OECT-based logic circuits fabricated with the proposed approach emerge with a high ON/OFF ratio (10^3 - 10^4) and remarkably fast switching response, reaching an ON/OFF ratio of >10^3 in 4-8 ms, which is further demonstrated by a propagation delay time of just above 1 ms in OECT-based logic inverter circuits operated at a frequency of 100 Hz. All-printed monolithically integrated OECT-based five-stage ring oscillator circuits further validated the concept with a resulting self-oscillation frequency of 60 Hz.

1. Introduction

Printed Electronics (PE) enables the manufacturing of cost- and material-efficient electronic devices and systems on various flexible large-area substrates, *e.g.*, paper, plastic, and textile.[1, 2] This has paved the way for the development of a variety of novel electronic devices that can be used in a broad range of application areas, *e.g.*, distributed healthcare, Internet of Things (IoT) and optoelectronics.

Standard fabrication techniques, such as screen, inkjet, gravure and, more recently, aerosol jet printing (AJP), are continually expanding the number of applications at a remarkable rate. In the field of PE, these deposition techniques have been used for fabrication and integration of digital logic circuits,[3] displays[4, 5] and sensors[6] on flexible substrates.

Nowadays, most electronic gadgets comprise integrated circuits containing transistors, the key active components of modern electronics. Synthesis of novel organic materials has fostered the development of organic transistors controlled via electrolytic interfaces: (i) organic electrochemical transistors (OECT) and (ii) electrolyte-gated field-effect transistors (EGOFET); two devices that are governed by different operation mechanisms, partly originating from the features of the organic semiconductors used as channel materials.[7] In the OECT, charges are contained in the entire bulk of the organic semiconductor, giving rise to the high volumetric capacitance, resulting in high on-currents, high transconductance, high ON/OFF ratio, simplified device architectures, and low operation voltages of approximately 1 V. However, the enormous device capacitance also results in slow transistor response; this can be explained by the fact that the OECT relies on the movement of ions from the electrolyte into the bulk of the channel, and vice versa. Conversely, in EGOFETs, charges accumulate at the interface between the semiconductor and the electrolyte due to the electric double layers, resulting in shorter switching time, equally low switching voltages, similar ON/OFF ratio, but clearly lower current throughput.[8, 9]

Emerging application areas for organic transistors, especially OECTs, are biosensing,[10, 11] electrophysiological recording,[12] neuromorphic devices[13] and printed circuits.[3] The thickness of the electrolyte layer is non-critical from a device functionality point of view. In screen printed devices, the electrolyte thickness typically exceeds 10 µm, thereby paving the way for robust device architectures empowering large-scale manufacturing via reliable printing techniques.[14]

An OECT is a three terminal device in which the source and drain electrodes are electronically connected via an organic semiconducting channel material, and a gate electrode is ionically linked to the channel by the electrolyte. Poly(3,4-ethylenedioxythiophene) doped with

poly(styrene sulfonate) (PEDOT:PSS) is commonly used as the organic conjugated polymer in printed OECT channels.[15]

Various OECT device architectures and materials have been explored in the last decade to improve the OECT switching response. As a result, by replacing PEDOT:PSS with carbon as the source and drain electrodes, short switching times and symmetric switching behavior have been reported in printed OECTs relying on PEDOT:PSS-based channels.[16] In 2017, this OECT architecture was used in a report covering the first fully screen printed digital circuits relying on vertically stacked OECTs.[17] Recently, large-scale integrated circuits including more complex screen printed OECT-based logic circuits with high ON/OFF ratio (>10^3) and short switching times (20-30 ms) were reported.[3] In 2021, fully screen printed OECT-based inverters and three-stage ring oscillators were demonstrated. A propagation delay of ~12 ms (with proper V_{OUT} voltage levels) was obtained for the inverters, while an oscillation frequency of ~20 Hz and a propagation delay of ~7 ms were achieved for the ring oscillators.[18] Hence, fully screen printed PEDOT:PSS-based OECTs and logic circuits have been reported previously, however, not combined with the AJP technique that herein leads to a new OECT manufacturing approach, as evidenced by inverters and five-stage ring oscillators with remarkable switching characteristics.

Improving the performance of the OECTs is associated with materials, fabrication techniques and device architectures.[3, 16-18] With the use of appropriate fabrication methods, crucial features and design flexibility can be achieved; in OECTs, it is in particular the reduction of area and thickness of the channel material that is important to enable shorter switching times. The AJP technique demonstrates the fabrication of highly precise and complex patterns, where feature sizes of 10 - 20 µm have been achieved.[19, 20] This allows for utilization in a large variety of devices and applications on both planar and non-planar substrates, *e.g.*, biosensors and integrated circuits.[21, 22]

The team of C. Daniel Frisbie was the first to explore the potentiality of AJP, alone or in combination with other techniques, *e.g.*, photolithography[22, 23] and stencil printing,[24] in the manufacturing of ion gel electrolyte-gated transistors (EGT). In 2010, in one of the pioneering works, they demonstrated the possibility of combining standard photolithography (electrode patterning) with AJP in the manufacturing of P3HT-based ion gel electrolyte-gated transistors with $<10^{-10}$ A OFF-current levels and short switching time of 1.3 ms (for a channel length of 10 µm).[22] In 2014, the same team further developed this work by evaluating the performance of EGTs utilizing aerosol jet printed source and drain electrodes and by demonstrating the

manufacturing of circuits (*e.g.*, ring oscillator and inverter) relying on p- and n-type semiconducting channel materials.[25, 26]

Here, we demonstrate fast and flexible manufacturing of OECTs with vertically stacked gate electrodes via a combination of screen and aerosol jet printing (SP and AJP) techniques. The proposed fabrication approach takes advantage of the reliability and speed of the well-established screen printing technology and high resolution of the AJP technique. Both area (width and length) and thickness of the channel material are crucial for the switching performance of OECTs since the current flow occurs in the entire bulk of the channel. Hence, the resolution and thickness of printed OECT channels deposited via both screen and AJP techniques have been evaluated in this work. The AJP of ~15 µm wide channels resulted in a substantial reduction of the channel volume as compared to the OECT channels deposited via conventional screen printing. Consequently, the reduced channel volume implies shorter transistor switching times, *i.e.*, the OFF-to-ON and ON-to-OFF switching time corresponds to ~16 ms and ~4 ms, respectively. In addition, the AJP devices exhibit high ON/OFF ratios of >25,000 and >10,000 (two different geometries and volumes of the AJP channels) as well as lower switching voltages, as evidenced by that an input voltage window of 1 V could be used, thereby ensuring longer operational lifetime. Moreover, OECT-based logic inverter circuits were operated at 100 Hz with propagation delays of ~1.2 ms, which is a significant improvement as compared to previously reported attempts.[3, 17, 18] All-printed five-stage ring oscillator circuits further validated the manufacturing approach with a self-oscillation frequency of ~60 Hz and a propagation delay per stage of ~1.7 ms. Therefore, this manufacturing approach allows for the printing of OECT-based logic circuits on flexible substrates and creates a path to other applications where the robustness of screen printing and the high resolution of AJP can be utilized.

2. Results

2.1. Use of different printing techniques for the fabrication of organic electrochemical transistors (OECTs)

Different deposition techniques can be used to provide deposited layers with different characteristics in terms of thickness and critical dimensions. The selection of the deposition method is a key to achieve design flexibility and improved device switching performances.

To prove this, a series of OECTs were printed. The OECT channels were deposited either by screen or aerosol jet printing, and the remaining OECT layers were deposited by screen printing.

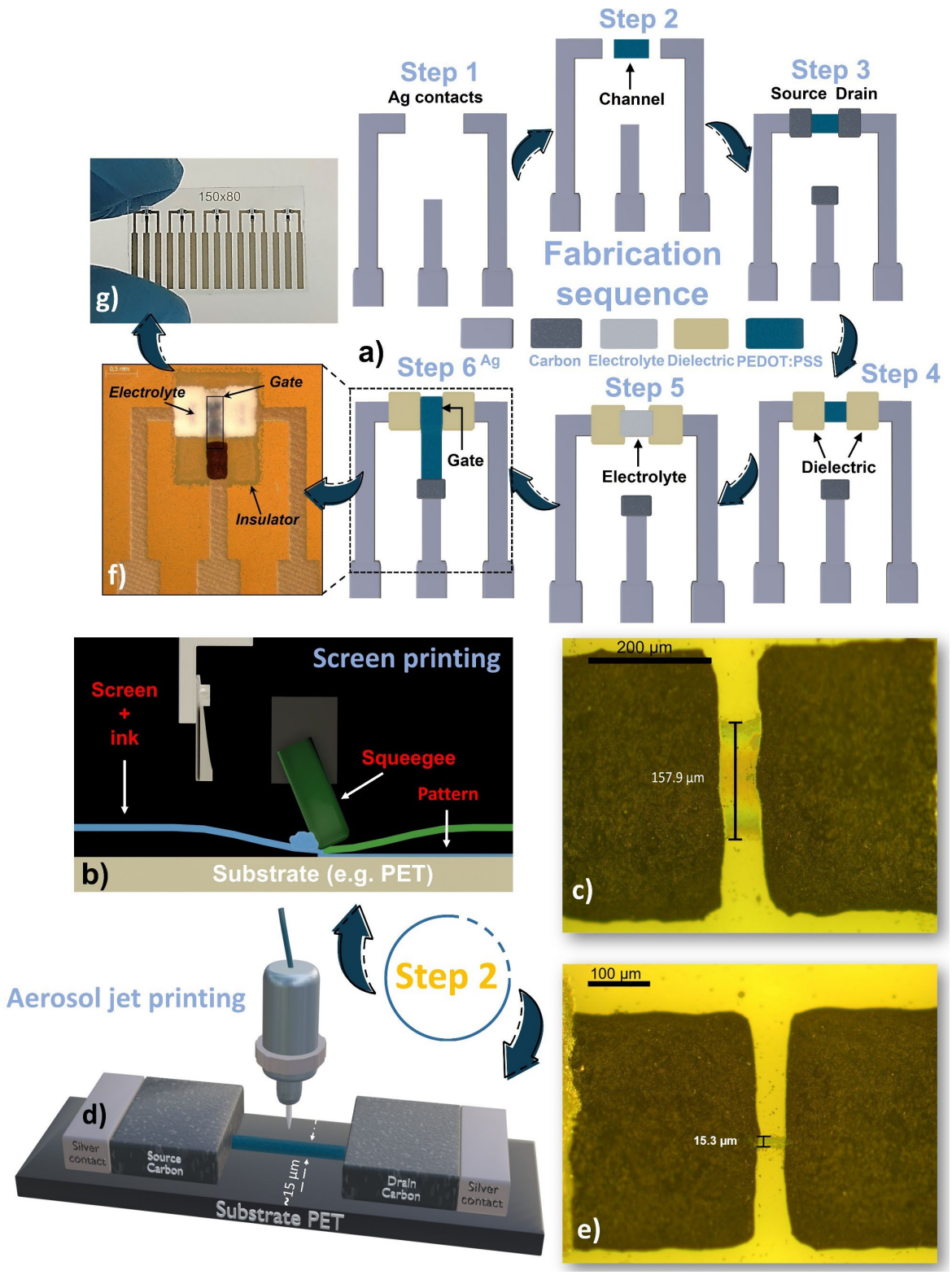

Figure 1. Illustration of the fabrication sequence and the different layers deposited via various printing techniques. a) The steps and schematics of the manufacturing process are described. b-e) Description of step 2 of the manufacturing process: the deposition of the OECT channel between the carbon-based source and drain electrodes; b) and c) show the schematic and the corresponding optical microscope image of a screen printed OECT channel, while d) and e) show the schematic and the corresponding

microscope image of an aerosol jet printed OECT channel. f) An optical microscope image showing various printed layers in one of the OECTs. g) A photograph showing a set of OECTs printed on a PET substrate.

The screen printed channels were used as a reference to benchmark the performances of the OECTs developed by SP and AJP techniques. The sole use of screen printing for OECT manufacturing has been widely explored by RISE, and in-depth analyses of this technology can be found in previous reports.[14, 16, 18, 27]

The manufacturing of the OECT device comprises six deposition steps (**Figure 1**a). More specifically: printing of Ag-based interconnects and contact pads (step 1), deposition of the PEDOT:PSS-based channel and gate electrodes (steps 2 and 6), printing of the carbon-based source and drain electrodes (step 3), deposition of an insulating layer (step 4) and an electrolyte layer (step 5). These steps are followed by an optionally printed insulating layer to provide mechanical protection of the final device (Figure 1f). In order to implement the envisaged variation in the geometrical properties of the channels (*e.g.*, width, length and thickness), step 2 of the process was performed by using either screen or aerosol jet printing techniques (Figure 1b and 1d). As clearly shown in Figure 1c and 1e, the PEDOT:PSS-based channels deposited with the two different techniques showed significantly different channel widths; those manufactured by aerosol jet printing were approximately one order of magnitude narrower. The resulting OECTs, in which the different printed layers have been deposited via a combination of SP and AJP techniques, are shown by the optical microscope image in Figure 1f and the photograph in Figure 1g.

The estimated mean volumes of the OECT channels (**Table 1**) – defined by the mean values of the width (W), length (L) and thickness (t) – were evaluated and correlated to the key characteristics of the resulting devices. Moreover, variations and limitations in printing resolution and channel thickness, with respect to each printing technique, were explored.

In devices denoted *Fully SP*, the channel was screen printed, while in the *SP + AJP large*, *SP + AJP medium* and *SP + AJP small* versions, the channels were fabricated by aerosol jet printing. The latter three sets of OECT devices (SP + AJP) were having different W, L and t, thus *large*, *medium* and *small* refer to the difference in channel volume, see Table 1.

To investigate the effect of the channel design on the OECT key switching characteristics, the four different OECT channel geometries were characterized via transfer measurements (**Table 2** and **Figure 2**a). The dynamic measurements were performed for two of these OECT versions (*SP + AJP large* and *small*), to evaluate the difference in switching time (Figure 2b) between the largest and smallest channel volumes (Table 1) and to show the reproducibility of the printed

devices (Figure 2c and 2d). Hence, these measurements provided the key parameters for the evaluation of standalone OECTs: switching time, switching voltage, transconductance, ON and OFF drain current values ($I_{D, ON}$ and $I_{D, OFF}$) and ON/OFF ratio ($I_{D, ON}/I_{D, OFF}$).

Table 1. Features of all-printed OECTs.

	Fully SP	***SP + AJP large***	***SP + AJP medium***	***SP + AJP small***
	Mean ± SD	Mean ± SD	Mean ± SD	Mean ± SD
Width (W), µm	**158.2** ± 3.3	**20.6** ± 1.2	**17.5** ± 0.8	**14.6** ± 0.4
Length (L; source-drain separation), µm	**89.6** ± 2.6	**86.5** ± 1.1	**87.3** ± 3.1	**70.3** ± 4.3
Thickness (t), µm	~0.5 [14]	~0.56	~0.42	~0.31
Estimated volume, µm³	~7,080	~500	~320	~160

While the $I_{D, OFF}$ and $I_{G, OFF}$ current levels recorded for all three versions of SP + AJP OECTs were comparable (~30-40 nA), appreciable differences were observed for the gate voltages at which the channels are fully depleted ($V_{G, OFF}$) for both SP + AJP and fully screen printed OECTs; decreased channel volume resulted in lowered $V_{G, OFF}$: 1.24 ± 0.02 V (*Fully SP*), 1.16 ± 0.02 V (*SP + AJP large*), 1.18 ± 0.008 V (*SP + AJP medium*) and 1.12 ± 0.02 V (*SP + AJP small*). The impact of the channel geometry and volume can be better appreciated by comparing $I_{D, ON}$ current levels and transconductance of the OECTs, which are 357 ± 34.5 µA and 1.1 ± 0.09 mS for the *SP + AJP small* device, 656 ± 55.9 µA and 2.7 ± 0.17 mS for the *SP + AJP medium* device, and 921 ± 25.5 µA and 3.9 ± 0.36 mS for the *SP + AJP large* device; the latter corresponds to ~190 S m^{-1}.

Table 2. Key characteristics extracted from the transfer sweeps from a set of printed OECTs of each geometry.

	Fully SP	***SP + AJP large***	***SP + AJP medium***	***SP + AJP small***
	Mean ± SD	Mean ± SD	Mean ± SD	Mean ± SD
$-I_{D, ON}$ (µA)	**415** ± 38.5	**921** ± 25.5	**656** ± 55.9	**357** ± 34.5
$-I_{D, OFF}$ (nA)	**46** ± 4.3	**36.3** ± 5.2	**29.3** ± 5.2	**35.3** ± 4.6
$V_{G, OFF}$ (V)	**1.24** ± 0.02	**1.16** ± 0.02	**1.18** ± 0.008	**1.12** ± 0.02
$I_{G, OFF}$ (A)	**40.5** ± 5.7	**43** ± 4.2	**32.3** ± 3.8	**34.3** ± 3
$-I_{D, ON}/-I_{D, OFF}$	**8,989** ± 274	**25,923** ± 3,885	**22,985** ± 3,809	**10,194** ± 576

Figure 2b shows the dynamic measurements recorded for two of the SP + AJP OECTs at 5 Hz. As can be seen, the major difference between the two OECT types lies in that different ON/OFF

ratios are obtained; ~9,800 and ~5,800 for the *SP + AJP large* and *SP + AJP small* devices, respectively.

Further data analysis also highlighted a difference in switching time. For the device *SP + AJP large*, a switching time from OFF-to-ON (switching from 10 to 90 % of the I_D maximum value) of ~32 ms was recorded, while the switch from ON-to-OFF (switching from 90 to 10 % of the I_D maximum value) required ~8 ms. For the device *SP + AJP small*, the OFF-to-ON switching time was ~16 ms, while the device switched from ON-to-OFF in ~4 ms. It should be noted that 4 ms is the minimum sampling interval of the measurement system in this case.

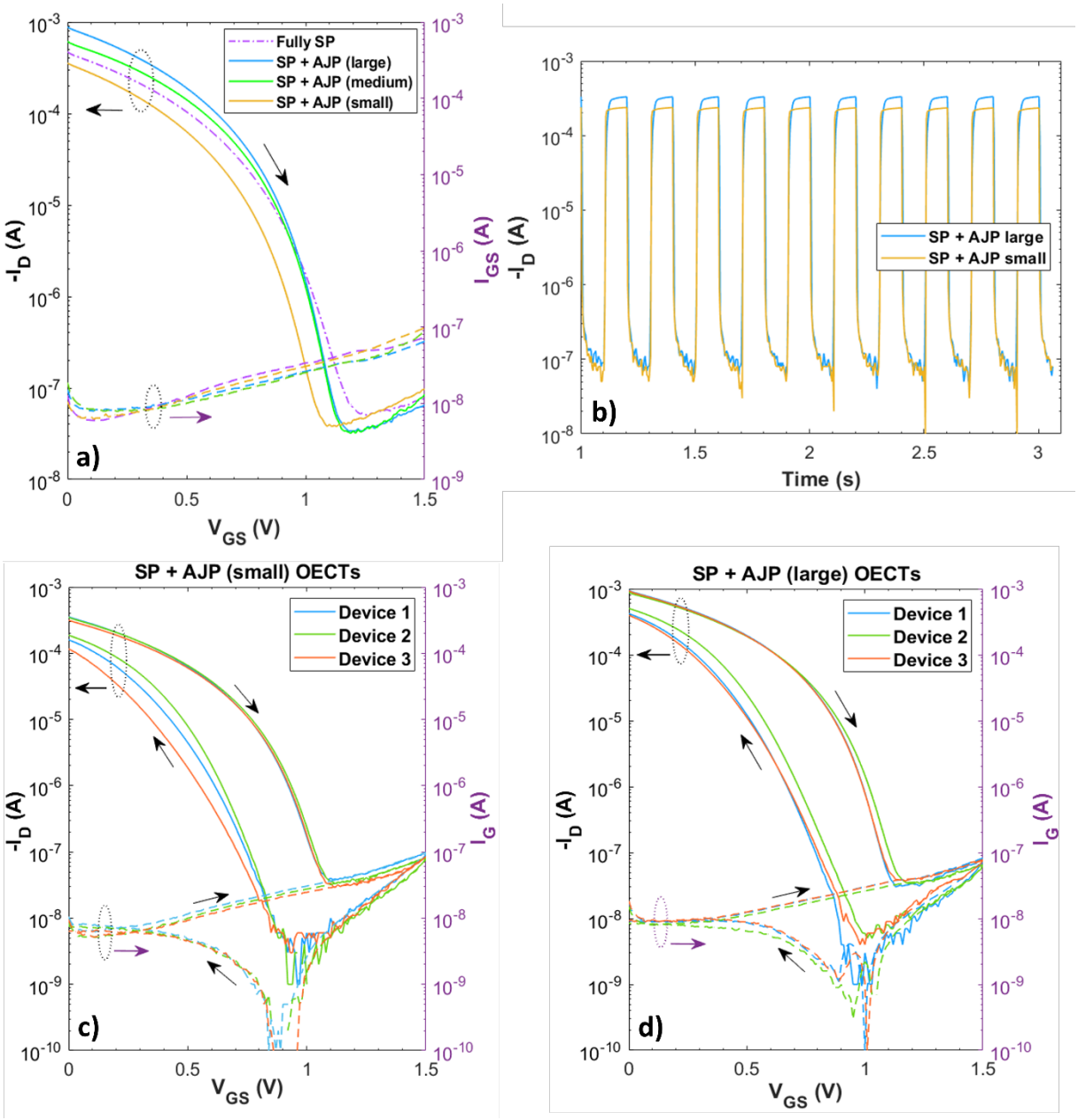

Figure 2. Transfer and dynamic characteristics of OECTs fabricated via different printing techniques. a) Transfer characteristics of screen printed OECTs having either screen or aerosol jet printed channels. The devices *SP + AJP large*, *SP + AJP medium* and *SP + AJP small* denote OECTs with aerosol jet printed channels with different volumes, while the *Fully SP* device is a fully screen printed OECT. b) Dynamic characteristics of two of the devices with aerosol jet printed channels. c) Transfer sweeps originating from three different OECTs manufactured according to the *SP + AJP small* device architecture. d) Transfer sweeps originating from three different OECTs manufactured according to the *SP + AJP large* device architecture.

2.2. OECT-based logic inverter fabricated by the combination of screen and aerosol jet printing

The inverter circuit is a fundamental building block used in many logic gates and digital circuits, and screen printed OECT-based inverters have been reported previously.[3, 17-18] However, there is still room for improvement of the switching performance of these inverters in order to enable even more applications. The OECT switching time is governed by several parameters, where the capacitance between the gate electrode and the channel plays a significant role. Hence, decreasing the volume of the channel will inevitably result in shorter OECT switching time due to the lowered device capacitance. This will, in turn, shorten the propagation delay in inverters and thereby also improve the switching performance in more advanced logic circuits containing a number of cascade-coupled inverters. From the dynamic measurements (Figure 2b) reported in section 2.1, the *SP + AJP small* OECT version exhibited the shortest switching time. Therefore, this version was further utilized for the fabrication of SP + AJP inverters and ring oscillators.

It is crucial to match the logic input voltage signal (V_{IN}) and the output voltage levels (V_{OUT}) to enable logic propagation in printed circuits. Additionally, upon increasing the frequency, *e.g.*, from 10 to 100 Hz, may cause changes in the propagation delay when comparing the HIGH and LOW V_{OUT} levels. When the V_{OUT} signal transits from the LOW state (HIGH state) to the HIGH state (LOW state), or vice versa, and reaches 50 % of the V_{IN} voltage window, it is denoted as tpLH and tpHL, respectively. The propagation delay of the inverter circuit is defined as the average value of tpLH and tpHL.

In a first approach, the inverter circuit (**Figure 3**a and 3b) was created by using *SP + AJP small* OECTs in conjunction with discrete resistors connected on a breadboard to allow for reconfiguration of the resistor values. The inverter circuit relies on voltage division in the resistor ladder, where the resistor values and the supply voltage levels define the V_{OUT} levels.

The V_{IN} signal is connected to the gate electrode of the OECT, thereby defining the conduction state of the OECT channel. The inverted V_{OUT} signal will toggle between two well-defined voltage levels by carefully selecting resistor values and supply voltages. The following values were used for the resistors connected on a breadboard to target a V_{OUT} window ranging between ~0 V and ~1 V: R1 = 40.7 kΩ, R2 = 18.4 kΩ and R3 = 47 kΩ. The dynamic response of the inverter, shown in Figure 3d and 3e, reveals that the digital LOW and HIGH output voltages when applying a square wave V_{IN} signal alternating between 0 and 1 V at a switching frequency of 10 Hz are lower than 0.005 V and higher than 0.9 V, respectively, while the V_{OUT} levels are ranging between 0.01 V and 0.9 V for V_{IN} oscillating at 100 Hz. The resulting signal propagation delays of this inverter are 1.85 ms and 1.2 ms at 10 Hz and 100 Hz, respectively.

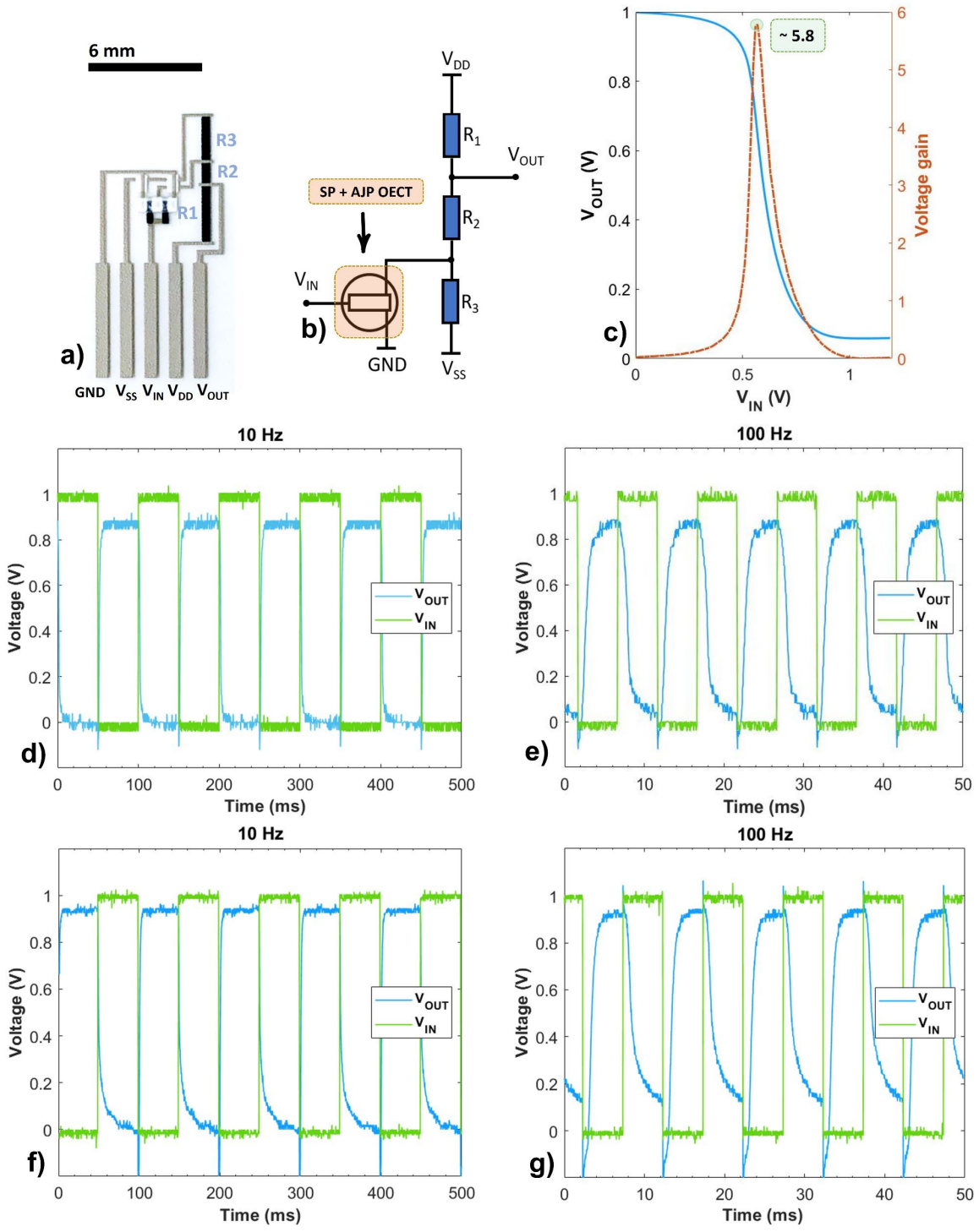

Figure 3. Switching response of all-printed inverters fabricated via the combination of screen and aerosol jet printing techniques. a-b) Photograph and schematic illustrating the all-printed OECT-based inverters. c) Voltage transfer characteristics of an SP + AJP inverter. Switching characteristics of d-e) an inverter that relies on the SP + AJP OECT and discrete resistors connected via a breadboard and f-g) an all-printed OECT-based inverter circuit. V_G was applied at a frequency of either 10 Hz (d and f) or 100 Hz (e and g).

In a second approach, the *SP + AJP small* OECT-based inverter was instead created through monolithic integration with printed resistors having the values R1 ~280 kΩ, R2 ~106 kΩ and R3 ~224 kΩ (Figure 3f and 3g**)**, thereby targeting V_{OUT} levels of ~0 V (digital LOW) and ~1 V (digital HIGH). These inverters were characterized by applying a square wave V_{IN} signal varying between 0 and 1 V at 10 and 100 Hz. At 10 Hz, as shown in Figure 3f, the recorded LOW and HIGH V_{OUT} levels are lower than 0.005 V and higher than 0.965V, while a V_{OUT} voltage window ranging between 0.1 V and 0.962V was recorded at a V_{IN} frequency of 100 Hz (Figure 3g). The signal propagation delays of the all-printed inverter are 1.55 ms at 10 Hz and 1.1 ms at an operating frequency of 100 Hz, for a V_{IN} voltage window ranging between 0 and 1 V, *i.e.*, the propagation delays are similar when comparing the two approaches. In contrast, the values demonstrated in previous reports exhibited propagation delays of ~50 ms[3] and more recently ~12 ms[18] with a maximum operation frequency of 10 Hz. Further analysis of the dynamic response in all-printed inverters after cycling for 60 seconds can be seen in the Supporting Information (Figure S1). Moreover, the switching time was also extracted from the 10 to 90 % (LOW to HIGH) and 90 to 10 % (HIGH to LOW) switching of the output voltage signal of the all-printed inverter,[28] which resulted in a switching time of ~4.5 ms and ~10 ms, respectively, at an operational frequency of 10 Hz. The noise margin (NM), based on the voltage transfer characteristics of the inverter, was estimated to ~14 % with a peak voltage gain of ~5.8 (Figure 3c). It should be noted that NM values up to ~18 % have been recorded, but at slightly lower gain. These values are comparable to those previously reported for fully screen printed OECT-based inverters[27] and indicate that SP + AJP OECT-based inverters can tolerate certain levels of noise in both logic states.

2.3. All-printed five-stage ring oscillator

A ring oscillator circuit was designed and manufactured to demonstrate the applicability of the proposed all-printed inverter in more complex circuitry. A ring oscillator circuit is created by cascade-coupling an odd number of inverters, where the output signal of the last stage is fed back to the input of the first inverter stage in the chain. Here, a five-stage ring oscillator is printed to demonstrate the concept. The proposed device also allows for an estimation of the average propagation delay. OECTs with the *SP + AJP small* architecture were implemented in the ring oscillator design. A photograph of a fully printed five-stage ring oscillator is shown in **Figure 4**a. The circuit self-oscillates upon applying the supply voltages to the resistor ladders of the inverters, hence, no input signal to the first inverter stage in the chain is required. As shown in Figure 4b, the LOW and HIGH output voltage levels are 0.32 V and 0.80 V. However,

despite the deviation from the targeted V_{OUT} values (0 V and 1 V), the all-printed ring oscillator is nevertheless capable of reaching distinct logic levels at a very high oscillation frequency; the average period time is 16.6 ms, which implies a self-oscillation frequency of ~60 Hz and a propagation delay of 1.66 ms. The V_{OUT} levels of all-printed inverters after oscillating for a longer time can be seen in Figure S2.

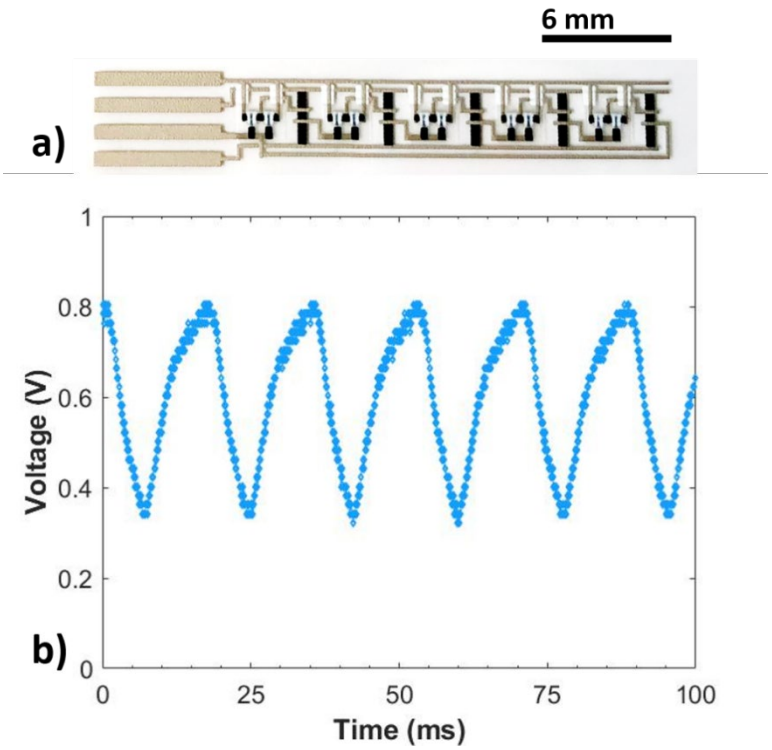

Figure 4. All-printed monolithically integrated five-stage ring oscillator fabricated via the combination of screen and aerosol jet printing techniques. a-b) Photograph and the output voltage levels of an all-printed five-stage ring oscillator originating from PEDOT:PSS-based OECTs with a W/L ratio of 15 µm/80 µm. Positive (VDD) and negative (VSS) supply voltages of 3.9 V and -4.14 V, respectively, were applied to the resistor ladder.

3. Discussions and Conclusions

The inherent feature of an OECT to transport charges within the complete bulk of the channel material makes the volume of the channel, and consequently the thickness combined with the lateral dimensions, critical for the resulting switching performance of the device, as evidenced by the results in the previous section. In this work, we are demonstrating all-printed OECTs with enounced performances that meet the requirements for many printed circuit applications in terms of short switching times.

This has been achieved by taking advantage of two different printing technologies, thereby bridging the versatility and robustness of screen printing with the high resolution (~10-20 µm)

of aerosol jet printing. In the proposed novel fabrication approach, all the layers except the PEDOT:PSS-based channel were reliably screen printed, while aerosol jet printing was used to print the active channel material at different geometries and thicknesses.

The use of aerosol jet printing allowed for significant changes of the geometrical dimensions of the channel, namely width and thickness, thereby the estimated channel volume was reduced by a factor of ~40, as compared to screen printed OECT channels, see Table 1. Hence, the overall device capacitance was lowered, which in turn is expected to result in faster switching response. This is demonstrated through measurements of standalone OECTs, all-printed OECT-based inverters and all-printed ring oscillator circuits consisting of five inverters connected in series. As shown in Figure 2b, standalone OECTs with AJP channels show almost full current modulation (ON/OFF ratio $>10^3$) within ~4-8 ms for both switching directions upon applying a square wave gate voltage signal, which is an improvement in comparison with OECTs having screen printed channels (20-225 ms).[14] In addition to this, the transfer characteristics show consistent switching behavior and low $V_{G,\,OFF}$ levels; the former ensures reliable propagation of the logic signal through more advanced all-printed logic circuits and the latter could result in extended operational lifetime due to the lowered voltage strain. The voltage strain is defined as the voltage difference between the gate and drain voltages (V_{GD}) during operation of OECTs and OECT-based logic circuits, and improper inverter design in combination with high $V_{G,\,OFF}$ amplitude may lead to V_{GD} values exceeding 3 V, which in turn results in severe parasitic side reactions due to the hygroscopic behavior of the electrolyte. Hence, an OECT architecture that exhibits low $V_{G,\,OFF}$ is critical to suppress the contribution from parasitic reactions, and this is obtained in the reported devices due to the thin AJP channels, thereby simplifying ion transport throughout the complete bulk of the channel material.

The characteristics of the SP + AJP printed inverters are shown in Figure 3. Here, an oscilloscope was used to record the V_{IN} and V_{OUT} signals to ensure sufficiently high sampling rate. The propagation delay of an inverter is an important parameter since it determines the maximum operational frequency of the logic circuit. The OECT manufacturing approach developed herein results in inverter propagation delays just above 1 ms, and adequate V_{OUT} levels are reached even upon providing the V_{IN} signal at 100 Hz. This is a remarkable result that further advances the all-printed OECT technology, especially considering that the electrolyte layer is screen printed and UV-cured, thereby resulting in a much lower ionic conductivity in comparison with aqueous salt solutions and ionic liquids often used in conjunction with OECTs manufactured by photolithography in the literature.

To further demonstrate the manufacturing approach and elaborate more on the topic of propagation delay, five-stage ring oscillators were monolithically integrated onto the flexible substrate. Each ring oscillator comprises five cascade-coupled inverters, where V_{OUT} of the last inverter stage is connected in a feedback loop to the input of the first inverter in the chain, hence, no external V_{IN} signal is required. The ring oscillator shown in Figure 4 was self-oscillating at a frequency of ~60 Hz, corresponding to a propagation delay of 1.66 ms. In other words, the propagation delays obtained for standalone inverters (1.1 ms at 100 Hz and 1.55 ms at 10 Hz) and ring oscillators (1.66 ms) are relatively similar, which is an important result showing the possibility to use OECT-based inverters in more advanced cascade-coupled logic circuits.

Finally, it should be mentioned that the switching times of the standalone OECTs (Figure 2) and the propagation delays of inverters (Figure 3) and ring oscillators (Figure 4) are deviating. At a first glance, this may seem contradictory since the very same SP + AJP OECT architectures are used throughout the report. However, this is explained by that the switching time of standalone OECTs is determined by full current modulation (ON/OFF ratio $>10^3$ of the channel). This switching time criterion is more difficult to fulfil, and thereby requires longer time as compared to the propagation delay obtained in inverters and ring oscillators; the circuits only require that a small portion of the full current modulation window (ON/OFF ratio >400) is reached in order to generate adequate voltage levels at the V_{OUT} measurement node.[3]

To the best of our knowledge, the reported values of the propagation delay (~1 ms at an operating frequency of 100 Hz) and the self-oscillation frequency (~60 Hz) of five-stage ring oscillator circuits are clearly beyond previously reported state-of-the-art all-printed OECT-based inverters and ring oscillators. Therefore, the achievements reported herein pave the way towards robust and reliable all-printed OECT-based logic circuits through the combination of screen and aerosol jet printing, with unprecedented switching performances in the resulting OECT devices and OECT-based logic circuits. The combination of these sheet-based printing techniques will bring flexibility and serve as a stepping stone from which various printed (bio)electronic applications will emerge, including OECT-based biosensors, devices for electrophysiological recording and logic circuits.

4. Experimental Section

Fabrication of OECTs via the combination of different printing techniques

The screen printing was performed using a DEK Horizon 03iX under ambient conditions (ca. 22 °C and 50 RH%). As depicted in Figure 1a, the fabrication of OECTs includes at least six printing steps to deposit the different layers. Plastic films (125 µm thick PET, Polifoil purchased from Policrom) were used as flexible substrates; prior to use, the plastic substrates were thermally stabilized by preheating in the oven for 30 min at 150 °C. Polyester-based screens with different mesh sizes (depending on the deposited layer) were acquired from Marabu Scandinavia AB and used in the screen printing process.

Step 1 – a commercially available silver paste (Ag 5000 from DuPont) was printed on the PET substrates to create interconnects and contact pads. Step 2 includes printing of the PEDOT:PSS-based channel. Different PEDOT:PSS inks were used depending on the ink requirement for the respective deposition technique: screen printing (Clevios S V4 screen printing paste from Heraeus) and aerosol jet printing (P JET 700N ink for inkjet printing from Heraeus). Before depositing the channel via aerosol jet printing, the inkjet ink (P JET 700 N) was ultrasonicated for 15 min and then filtered via a 0.45 µm syringe filter (Acrodisc®) with a PVDF membrane to disperse the ink and remove particle agglomeration. To achieve 15 µm line width, a nozzle diameter of 150 µm was used for the aerosol jet printing process. Microscope images of the OECT channels, fabricated via different printing techniques, are shown in Figure 1c and 1e.

Step 3 - a carbon paste (7102 from DuPont) was used to deposit the source and drain electrodes and establish electrical contacts with the silver.

Step 4 includes screen printing of an insulating layer (UVSF from Marabu); the purpose of this layer is to define the opening between the source and drain electrodes that, in turn, confine the subsequent screen printed electrolyte layer in Step 5. It should be noted that the insulating layer is optional, it is not needed for the OECT device functionality, but it may have a positive effect on the reproducibility of the device characteristics.

Step 5 - the electrolyte (E003 provided by RISE) layer was screen printed onto the PEDOT:PSS-based channels.

In Step 6, the gate electrode material (Clevios S V4 from Heraeus) was screen printed on top of the solidified electrolyte layer, forming vertically stacked OECTs. A magnified area of an all-printed OECT is shown by the microscope image in Figure 1f, while the photograph in Figure 1g shows a set of OECTs printed on the flexible PET substrate.

Steps 1-3 and 6 include annealing, either by using a conveyor belt oven (for the screen printed layers) or using a convection oven (for the aerosol jet printed layer) at 120°C after each printing step. Steps 4 and 5 are cured by UV light irradiation.

The geometry (width, length and thickness) of the printed layers have been estimated using an optical profilometer (PLU neox from Sensofar) and by using an optical microscope from Leica Microsystems. The resulting thicknesses of various layers printed on flexible PET substrates are the following: silver pads and interconnects 11 µm, carbon 9 µm, insulator 15 µm and electrolyte 13 µm. The thicknesses of the three sets of aerosol jet printed channels are ~0.31, ~0.42 and ~0.56 µm, while the screen printed channels are ~0.5 µm thick (with a roughness of 30 nm).[14] These thickness values were obtained by the optical profilometer, see Figure S3. The lengths of the OECT channels, defined by the distance between the screen printed source and drain electrodes, were 89.6 ± 2.6 µm, 86.5 ± 1.1 µm and 87.3 ± 3.1 µm for the *Fully SP*, *SP + AJP large* and *SP + AJP medium* OECTs, respectively, and 70.3 ± 4.3 µm for the *SP + AJP small* OECTs. The OECT channel widths are limited by the resolution of the respective printing technique being used; see Table 1 for further details. The volumes of the SP and AJP channels were estimated and provided as mean ± standard deviation (SD) values. To determine the mean and SD values, a set of OECTs comprising up to 5 devices was used for the respective design.

Electrical characterization

All the measurements were carried out under controlled conditions: ~22 °C and ~50 RH%. Electrical characterization of the devices was performed by transfer sweeps (I_D - drain current vs V_G - gate voltage) and dynamic measurements (I_D vs time). The transfer characteristics of OECTs and inverters were recorded by using a semiconductor parameter analyzer (HP/Agilent 4155B). The drain voltage (V_D) was set to -1 V, while the gate voltage was stepped from 0 V to 1.5V, and then back to 0 V, in incremental steps of 10 mV. Thus, $I_{D,\,ON}$ and $I_{D,\,OFF}$ denotes the drain current at an applied gate voltage of 0 V or 1.5 V, respectively. For the dynamic measurements, the parameter analyzer was used to record I_D vs time at a constant V_D of -1 V, while a function generator (Agilent 33120A) was used to provide V_G between 0 V ($I_{D,\,ON}$) and 1.5 V ($I_{D,\,OFF}$) for standalone OECTs, and V_G between 0 V and 1 V for the inverter circuits. A digital storage oscilloscope (DSOX1204G from Keysight) was used to record the input and output voltage levels from the all-printed circuits at higher resolution, while the parameter analyzer provided the supply voltages.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement No 813863 (BORGES) and the European Union´s Horizon 2020 research and innovation programme under the grant agreement No 825339 (WEARPLEX).

Conflict of Interest

Acreo AB filed a patent application related to the electrolyte used in this work, through the World Intellectual Property Organization, international publication number WO 2012/136781, filed on 5 April 2012, granted on 19 June 2018 with patent number US 10001690B2. P.A.E. filed a patent application via Acreo AB, through the World Intellectual Property Organization, international publication number WO 2011/042430, filed on 5 October 2010, granted on 19 August 2014 with patent number US 8810888B2. The other authors declare no competing interests.

References

[1] V. Beni, D. Nilsson, P. Arven, P. Norberg, G. Gustafsson, A. P. F. Turner, *ECS J. Solid State Sci. Technol.* **2015**, *4*, 10.

[2] M. Berggren, D. T. Simon, D. Nilsson, P. Dyreklev, P. Norberg, S. Nordlinder, P. Andersson Ersman, G. Gustafsson, J. J. Wikner, J. Hederén, H. Hentzell, *Adv. Mater.* **2016**, *28*, 10.

[3] P. Andersson Ersman, R. Lassnig, D. Tu, V. Keshmiri, R. Forchheimer, S. Fabiano, G. Gustafsson, M. Berggren, *Nat. Commun.* **2019**, *10*, 5053.

[4] P. Andersson, R. Forchheimer, P. Tehrani, M. Berggren, *Adv. Funct. Mater.* **2007**, *17*, 16.

[5] H. Zheng, Y. Zheng, N. Liu, N. Ai, Q. Wang, S. Wu, J. Zhou, D. Hu, S. Yu, S. Han, W. Xu, C. Luo, Y. Meng, Z. Jiang, Y. Chen, D. Li, F. Huang, J. Wang, J. Peng, Y. Cao, *Nat. Commun.* **2013**, *4*, 1971.

[6] Y. Khan, A. E. Ostfeld, C. M. Lochner, A. Pierre, A.C. Arias, *Adv. Mater.* **2016**, *28*, 22.

[7] L. Kergoat, B. Piro, M. Berggren, G. Horowitz, M. C. Pham, *Anal. Bioanal. Chem.* **2012**, *402*, 1813.

[8] D. Nilsson, T. Kugler, P. O. Svensson, M. Berggren, *Sens. Actuators B* **2002**, *86*, 193.

[9] J. Rivnay, S. Inal, A. Salleo, R. M. Owens, M. Berggren, G. G. Malliaras, *Nat. Rev. Mater.* **2018**, *3*, 17086.

[10] A. M. Pappa, V. F. Curto, M. Braendlein, X. Strakosas, M. J. Donahue, M. Fiocchi, G. G. Malliaras, R. M. Owens, *Adv. Healthcare Mater.* **2016**, *5*, 2295.

[11] L. Bai, C. G. Elosegui, W. Li, P. Yu, J. Fei, L. Mao, *Front. Chem.* **2019**, *7*, 313.

[12] D. Khodagholy, T. Doublet, P. Quilichini, M. Gurfinkel, P. Leleux, A. Ghestem, E. Ismailova, T. Hervé, S. Sanaur, C. Bernard, G. G. Malliaras, *Nat. Commun.* **2013**, *4*, 1575.

[13] P. Gkoupidenis, D. A. Koutsouras, G. G. Malliaras, *Nat. Commun.* **2017**, *8*, 15448.

[14] M. Zabihipour, R. Lassnig, J. Strandberg, M. Berggren, S. Fabiano, I. Engquist, P. Andersson Ersman, *npj Flex. Electron.* **2020**, *4*, 15.

[15] A. Elschner, S. Kirchmeyer, W. Lövenich, U. Merker, K. Reuter, *PEDOT: principles and applications of an intrinsically conductive polymer*, CRC press, Boca Raton **2010**.

[16] P. Andersson Ersman, D. Nilsson, J. Kawahara, G. Gustafsson, M. Berggren, *Org. Electron.* **2013**, *14*, 1276.

[17] P. Andersson Ersman, D. Westerberg, D. Tu, M. Nilsson, J. Åhlin, A. Eveborn, A. Lagerlöf, D. Nilsson, M. Sandberg, P. Norberg, *Flex. Print. Electron.* **2017**, *2*, 4.

[18] M. Zabihipour, D. Tu, J. Strandberg, M. Berggren, I. Engquist, P. Andersson Ersman, *Adv. Mater. Technol.* **2021**, *6*, 12.

[19] E. B. Secor, *Flex. Print. Electron.* **2018**, *3*, 2.

[20] A. Mahajan, C. D. Frisbie, L. F. Francis, *ACS Appl. Mater. Interfaces* **2013**, *5*, 11.

[21] D. Majak, J. Fan, S. Kang, M. Gupta, *J. Mater. Chem. B* **2021**, *9*, 2107.

[22] Y. Xia, W. Zhang, M. Ha, J. H. Cho, M. J. Renn, C. H. Kim, C. D. Frisbie, *Adv. Funct. Mater.* **2010**, *20*, 587.

[23] J. H. Cho, J. Lee, Y. Xia, B. Kim, Y. He, M. J. Renn, T. P. Lodge, C. D. Frisbie, *Nat. Mater.* **2008**, *7*, 900.

[24] W. J. Hyun, E. B. Secor, M. C. Hersam, C. D. Frisbie, L. F. Francis, *Adv. Mater.* **2015**, *27*, 1.

[25] K. Hong, S. H. Kim, A. Mahajan, C. D. Frisbie, *ACS Appl. Mater. Interfaces* **2014**, *6*, 18704.

[26] K. Hong, Y. H. Kim, S. H. Kim, W. Xie, W. D. Xu, C. H. Kim, C. D. Frisbie, *Adv. Mater.* **2014**, *26*, 7032.

[27] M. Zabihipour, D. Tu, R. Forchheimer, J. Strandberg, M. Berggren, I. Engquist, Peter Andersson Ersman, *Adv. Mater. Technol.* **2022**, 2101642.

[28] P. C. Hütter, T. Rothländer, A. Haase, G. Trimmel, B. Stadlober, *Appl. Phys. Lett.* **2013**, *103*, 043308.