High-gain Logic Inverters Based on Multiple Screen Printed Organic Electrochemical Transistors

Marzieh Zabihipour, Deyu Tu, Robert Forchheimer, Jan Strandberg, Magnus Berggren, Isak Engquist, and Peter Andersson Ersman*

M. Zabihipour, Dr. D. Tu, Prof. M. Berggren, Dr. I. Engquist

Laboratory of Organic Electronics, Department of Science and Technology, Linköping University, SE-60174, Norrköping, Sweden

Prof. R. Forchheimer

Division of Information Coding, Department of Electrical Engineering, Linköping University, Linköping SE-581 83, Sweden.

J. Strandberg, Dr. P. Andersson Ersman

RISE Research Institutes of Sweden, Printed, Bio- and Organic Electronics, Bredgatan 33, Box 787, SE-60117 Norrköping, Sweden

Prof. M. Berggren, Dr. I. Engquist

Wallenberg Wood Science Center, Linköping University, SE-60174 Norrköping, Sweden

E-mail: isak.engquist@liu.se

Keywords: novel inverter designs, tunable voltage gain, organic electrochemical transistors, printed organic electronics, PEDOT:PSS

Abstract

Organic electronic circuits based on organic electrochemical transistors (OECTs) are attracting great attention due to their printability, flexibility, and low voltage operation. Inverters are the

building blocks of digital logic circuits (e.g., NAND gates) and analog circuits (e.g., amplifiers). However, the utilization of OECTs in electronic logic circuits is challenging due to the resulting low voltage gain and low output voltage levels. Hence, inverters capable of operating at relatively low supply voltages, yet offering high voltage gain and also larger output voltage windows than the respective input voltage window are desired. Herein, inverters realized from PEDOT:PSS-based OECTs are designed and explored, resulting in logic inverter structures exhibiting high voltage gains, enlarged output voltage windows and tunable switching points. The inverter designs are based on multiple screen printed OECTs and a resistor ladder, where one OECT is the driving transistor while one or two additional OECTs are used as variable resistors in the resistor ladder. The performance of the inverters is investigated in terms of voltage gain, output voltage levels and switching point. We demonstrate inverters, operating at +/-2.5 V supply voltage and an input voltage window of 1 V, that can achieve an output voltage window with almost 110% increment and a voltage gain up to 42.

1. Introduction

Organic electrochemical transistors (OECT)[1–13,14] belong to a class of organic electronic devices which play a significant role in the field of printed electronics. Easy fabrication with low temperature processing techniques, such as screen printing[9,15–17], simplifies large scale production of flexible devices[18]. Thanks to low voltage operation[19], high transconductance[3,20] and simple design, OECTs have attracted great attention in recent years. Hence, OECTs are good candidates for variety of applications such as printed electronic circuits[6,15,16,18], different types of sensing and interfacing[10,21], neuromorphics[13,22] and wearable electronics[23,24]. In addition, electronic circuits based on OECTs, such as OECT-based logic gates[15] and printed logic circuits[16,18,25], are reported in the literature. In this context, OECT-based inverters[18,19,26]

enable the development of OECT-based integrated electronics[27] and bioelectronics[28]. However, incorporating OECTs in electronic circuits can be challenging due to generally low voltage gain[5,14,15,27–29] and lack of control over the output voltage window. Moreover, operating OECT-based inverters at a relatively low supply voltage is important for minimizing the power consumption of OECT-based circuits. Current studies that are based on inverters with OECTs that have one type of charge for their channel conduction (either an n- or p-type channel material), so called unipolar OECT inverters, include one single OECT in their structure to control the input signal[5,16,18,19]. The output levels and voltage gain strongly depend on resistances and supply voltages used in the inverter[19]. In OECT inverters especially based on low resistances in the resistor ladder, it is common that the output levels degrade after a few seconds of switching, which makes it difficult to obtain reliable signal propagation in circuits[19]. Therefore, obtaining an output window which is larger than the respective input window while using relatively small supply voltages is desired in applications. To achieve this, new OECT-based inverter designs are here proposed with extra OECTs as variable resistive load, inspired by various inverter designs of p-type-only organic field-effect transistors operated in enhancement-mode[30]. For example, an extra transistor either in saturation or diode configuration works[30] as a variable load. Given that the OECTs based on conducting polymer PEDOT:PSS are operated in depletion-mode and the inverter design requires a resistor ladder, we propose the OECT-based inverter designs consisting of variable loads with the feasibility to tune the key parameters, such as voltage gain and logic output levels. We thoroughly investigated the novel OECT-based inverter designs with various resistor ladders on breadboard. In addition, the selected designs are realized in a monolithically integrated manner with both printed OECTs and resistors. The performance of the new inverter designs is comprehensively evaluated in terms of voltage gain and output levels when using various resistor ladders and supply voltages. The proposed designs accomplished high voltage gain peak values and output windows larger than the corresponding input windows when using

resistances in the range of a few tens of kΩ and relatively low supply voltages. To the best of our knowledge, this is the first time that PEDOT:PSS-based OECTs are reported in printed inverters with high voltage gain and tunable switching points and output levels. This voltage tunability allows for inverters in new applications where the power supply is limited and high voltage gain is required.

2. Results and Discussion

2.1 Inverter performance metrics

In this study, the inverters are based on screen printed PEDOT:PSS OECTs that are operated in depletion mode with a channel dimension of 150x100 μm^2. **Figure 1a** and **1b** show the transfer characteristics of a printed OECT at drain voltages (V_D) of -0.1 V and -1 V, respectively, where the drain current (I_D) of a forward sweep is plotted for both linear (Figure 1a) and saturation (Figure 1b) regions when the gate voltage (V_G) is changing from -0.3 V to 1.3 V at a 10 mV/s step size. According to both Figure 1a and 1b, the printed OECT switches OFF at around $V_G \approx$ 1 V with an ON/OFF ratio of approximately five orders of magnitude. The transfer curve slope ($\partial I_D/\partial V_G$), also known as transconductance (g_m), is extracted from the I_D-V_G curves and illustrated by the red curves in Figure 1.

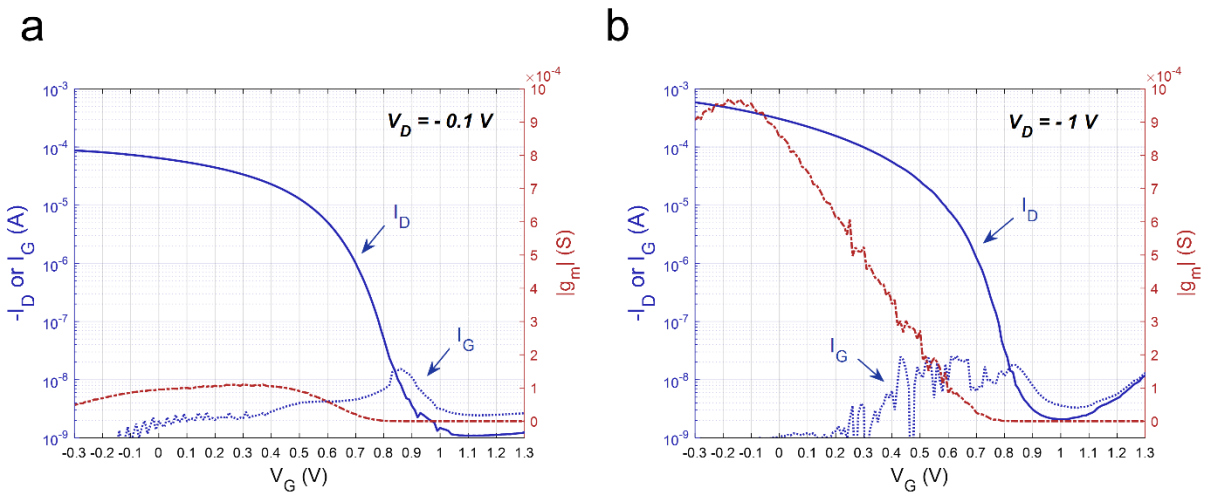

Figure 1: Transfer characteristics of a screen printed OECT with a channel area of 150x100 µm² at V_G = [-0.3/1.3] V and with (a) V_D = -0.1 V (linear region) and (b) V_D = -1 V (saturation region).

As Figure 1b shows, the g_m peak in the saturation region is located at around V_G = -0.15 V where there is relatively a large change in I_D (larger than it appears in Figure 1a; note the log scale). Figure 1a indicates that operating the OECT in the linear region leads to a g_m displaying a wider bell-shaped curve with a small peak (~100 µS) centered towards higher V_G values. In contrast, above V_G~ 0.8 V, where the channel is almost reduced to its non-conducting state, the g_m is nearly zero even though the I_D-V_G curve has a steep slope there in the subthreshold region. Comparison between Figure 1a and 1b shows that a higher g_m peak is obtained when the OECT operates at higher V_D. This is due to improved current modulation and enhanced signal amplification at elevated V_D values, which also implies that g_m is proportional to V_D in the linear region (at low V_D). Therefore, to achieve the highest g_m value, the OECT should be operated in its saturation region. However, here it should be noted that increased V_G levels, while operating the PEDOT:PSS-based depletion mode OECT in the saturation region (at elevated V_D), do not result in increased g_m values, since the g_m peak is obtained at V_G levels close to 0 V.

Despite many advantages and the popularity of PEDOT:PSS OECTs, the depletion-mode operation makes them quite unique in the application of digital logic circuits. Unlike enhancement-mode or complementary technologies, the inverter design of PEDOT:PSS-based OECTs typically consists of one transistor and three resistors, as shown in **Figure 2a**. This inverter structure is referred to as a standard or one transistor (1T) inverter. In this study, new inverter designs are developed based on the standard OECT-based inverter structure. One of the keys is to evaluate and compare their inverter performance based on three performance metrics: The output voltage (V_{OUT}) window, voltage gain and switching point. Below, we will describe each of these three metrics and their significance.

The **voltage gain** (A) is defined as the ratio of V_{OUT} to the input voltage (V_{IN}), $A=\partial V_{OUT}/\partial V_{IN}$. The voltage gain reflects the switching characteristics by showing the ability of the device to amplify a voltage signal from the input to the output. An inverter is set to operate with a particular set of voltage amplitudes, depending on its resistor ladder, supply voltage levels and the transistor operational behavior. In this context, the voltage gain is a measure of the ability of an inverter to increase the amplitude of a voltage signal from the input to the output port by adding energy converted from the power supply to the voltage signal. A high voltage gain reflects a high amplifying ability of the device. In the following, the voltage gain is derived and determined for 1T inverters.

The V_{OUT} can be written as a function of the current passing through the OECT (I_D):

$$V_{OUT} = V_+ - R_1 \frac{I_D + \frac{V_+ - V_-}{R_3}}{1 + \frac{R_1 + R_2}{R_3}} = \left(V_+ - R_1 \frac{V_+ - V_-}{R_1 + R_2 + R_3}\right) - \frac{R_1 R_3}{R_1 + R_2 + R_3} I_D \qquad (1),$$

where V_+ and V_- are the positive and negative supply voltages, respectively, and R_1, R_2, R_3 are the resistances of the resistor ladder (cf. Figure 2a).

The differential form of I_D can be expressed as[7]:

$$dI_D = g_m dV_G + g_d dV_D \quad (2),$$

where g_m is the transconductance and g_d is the drain conductance, and $V_G = V_{IN}$.

Based on Figure 2a, the relationship between V_D and V_{OUT} can be described as:

$$V_D = V_{OUT} - (V_+ - V_{OUT})\frac{R_2}{R_1} \quad (3).$$

From Equation (1), we have that

$$dV_{OUT} = -\frac{R_1 R_3}{R_1+R_2+R_3} dI_D \quad (4).$$

Using Equation (2) and (3) in Equation (4), the voltage gain A can be obtained as

$$A = \frac{\partial V_{OUT}}{\partial V_{IN}} = \frac{-\frac{R_1 R_3}{R_1+R_2+R_3} g_m}{1+\frac{R_3(R_1+R_2)}{R_1+R_2+R_3} g_d} \quad (5).$$

In the saturation region, where I_D is independent of V_D and hence g_d =0, Equation (5) can be simplified as

$$A = -\frac{R_1 R_3}{R_1+R_2+R_3} g_m \quad (6).$$

As Equation (6) states, in order to achieve high voltage gain, the resistance of the ladder and/or the g_m of the OECT can be increased. To increase the OECTs' transconductance, the capacitance per volume should be improved (i.e., enhancing the bulk doping) by changing the properties of the electrolyte or the active channel material, or by changing the OECT design. Increasing the load resistance results in higher voltage gain, however, at the cost of switching speed[19]. Since the g_m for PEDOT:PSS-based OECTs is typically high at lower V_G (Figure 1), to achieve a high voltage gain (Equation 6), there is a trade-off between the resistor ladder and the g_m. For instance, a smaller R_3 shifts the voltage gain peak to towards lower V_G, which corresponds to higher g_m, however, it reduces the load resistance and compromises the V_{OUT}

level of the digital 'HIGH' V_{OUT} level ($V_{OUT,H}$). A variable resistance of R_3 could alleviate this trade-off.

The **switching point** of an inverter is a V_{IN} value at which the voltage gain peak is observed. In order to run inverters as digital devices at low voltage, the switching point is an important parameter. For instance, in case of inverter or logic gate applications, the OECT in OECT-based inverters needs to operate at around the maximum g_m region which occurs at low V_G values. This means having the switching point as low as possible is desired. Throughout this work the V_{IN} value at which the voltage gain peak is observed is referred to as the 'switching point'.

The **V_{OUT} window** is defined as the difference between the $V_{OUT,H}$ and the digital 'LOW' V_{OUT} level ($V_{OUT,L}$). In an OECT-based inverter, $V_{OUT,L}$ is obtained at the V_{OUT} node by applying $V_{IN,H}$ to the OECT gate electrode, and vice versa. Ideal 1T inverter operation would be when the high and low levels of V_{IN} and V_{OUT} show identical values, i.e., obtaining restored input and output levels ($V_{IN,L} = V_{OUT,L}$ and $V_{IN,H} = V_{OUT,H}$). Digital circuits usually include several inverters in which the V_{OUT} levels of one inverter will be the V_{IN} levels for the next stage. In such sequential signal transmission from one inverter to the next one, if the V_{OUT} window shrinks after a few stages of signal propagation, the attenuated signal will eventually disable the inverters from switching. In such situations, the logic 'LOW' and 'HIGH' levels are too close to each other and cannot be differentiated by the inverters. Hence, to implement robust logic operation, the V_{OUT} window of the inverters needs to be of a certain size to assure the logic propagation between stages. For instance, a 1T inverter based on the R_1 = 57.6, R_2 = 19 and R_3 = 41 kΩ resistor ladder and the supply voltages +/-3 V will only give a V_{OUT} window of 0.65 V ($V_{OUT,L}$ = 0.07 V, $V_{OUT,H}$ = 0.72 V, based on simulations using a SPICE model[16]), which may not be sufficient to control the next logic stage of an inverter chain. The typical solution is to increase the supply voltage to +/-5 V. However, increasing the supply voltage has some drawbacks which are explained in the following. For a given resistor ladder and particular

V_{IN} levels, the drain side of the OECT in the 1T inverter experiences a specific voltage (V_{DS}). By increasing the supply voltage also results in increased V_{DS}. As a consequence, a high V_{DS} value can elevate the leakage current in the OECT OFF state and negatively affect the lifetime[19].

In 1T inverters, the resistance of the OECT channel in the ON (R_{ON}) and OFF (R_{OFF}) states plays a major role in the resistor selection[19]. Assuming $V_+ = -V_-$ and $R_{ON} << R_3 << R_{OFF}$, the V_{OUT} window of 1T inverters is derived as follows.

$$V_{OUT,H} = \frac{R_2}{R_1+R_2} V_+ \quad (7)$$

$$V_{OUT,L} = \frac{R_3+R_2-R_1}{R_1+R_2+R_3} V_+ \quad (8)$$

Based on Equation 7, R_1 needs to be relatively small to achieve a large $V_{OUT,H}$. For the same supply voltage V_+, Equation 8 suggests a relatively large R_1 to match the sum of R_2 and R_3. These requirements for R_1 are obviously not compatible, meaning that a compromise has to be found, and that further optimization of the logic V_{OUT} window would require a variable R_1 resistance in the resistor ladder. In general, R_1 would need to have a small value when aiming at a large $V_{OUT,H}$ and a significantly larger value when targeting an ideal $V_{OUT,L}$. Optimization of V_{OUT} would also be beneficial since the supply voltages (V_+ and V_-) can be reduced when a logic V_{OUT} window larger than the V_{IN} window is obtained, and this may open up new applications where the power supply is limited. It is also worth mentioning that by lowering the supply voltage the operational lifetime of OECT-based inverters will be extended[19].

2.2 Inverter structures

For the reasons given above, here a strategy is employed to improve the inverter performance in terms of voltage gain and logic V_{OUT} window, involving the use of a resistor and an OECT together to function as a variable resistor that replaces a fixed resistor in the resistor ladder. To

obtain the variable resistor, a resistor is connected between the gate and the source of an OECT, and when current is passing through the resistor a voltage bias is created at the gate of the OECT. Based on this concept, we will replace R_1 (2T-R_1 design) or R_3 (2T-R_3 design) or both R_1 and R_3 (3T design). The resulting inverter structures are schematically shown in Figure 2b-d. Hence, the standard inverter (1T design, Figure 2a) has only one OECT in the structure and the modified versions include one or two extra OECTs that are coupled with one or two of the resistors.

2.2.1 Inverters with variable resistor(s)

As discussed above, introducing variable resistors in the resistor ladder of inverters with PEDOT:PSS-based OECTs will improve the voltage gain and the V_{OUT} window, while lowering the required voltage supply. Here, a variable resistor as the building block is defined as the combination as a resistor and an OECT, where the resistor is connected between the gate and the source of the OECT, illustrated schematically in **Figure S1**. As Figure S1 shows, when current is passing through the resistor it creates a voltage (V_G) to the gate electrode of the OECT. By this, the gate electrode of the coupled OECT experiences a certain voltage range (referred to as V_G) which depends on the resistance and the drain current passing through the transistor channel, resulting in a variable resistance of the block. Throughout this work, the variable resistor block is applied to either R1, or R3, or both R1 and R3, as shown in Figure 2. For instance, inverters that comprise one variable resistor (2T designs) consist of two OECTs in total; one OECT is serving as the driving transistor and the other OECT is coupled with a resistor to function as a variable resistor.

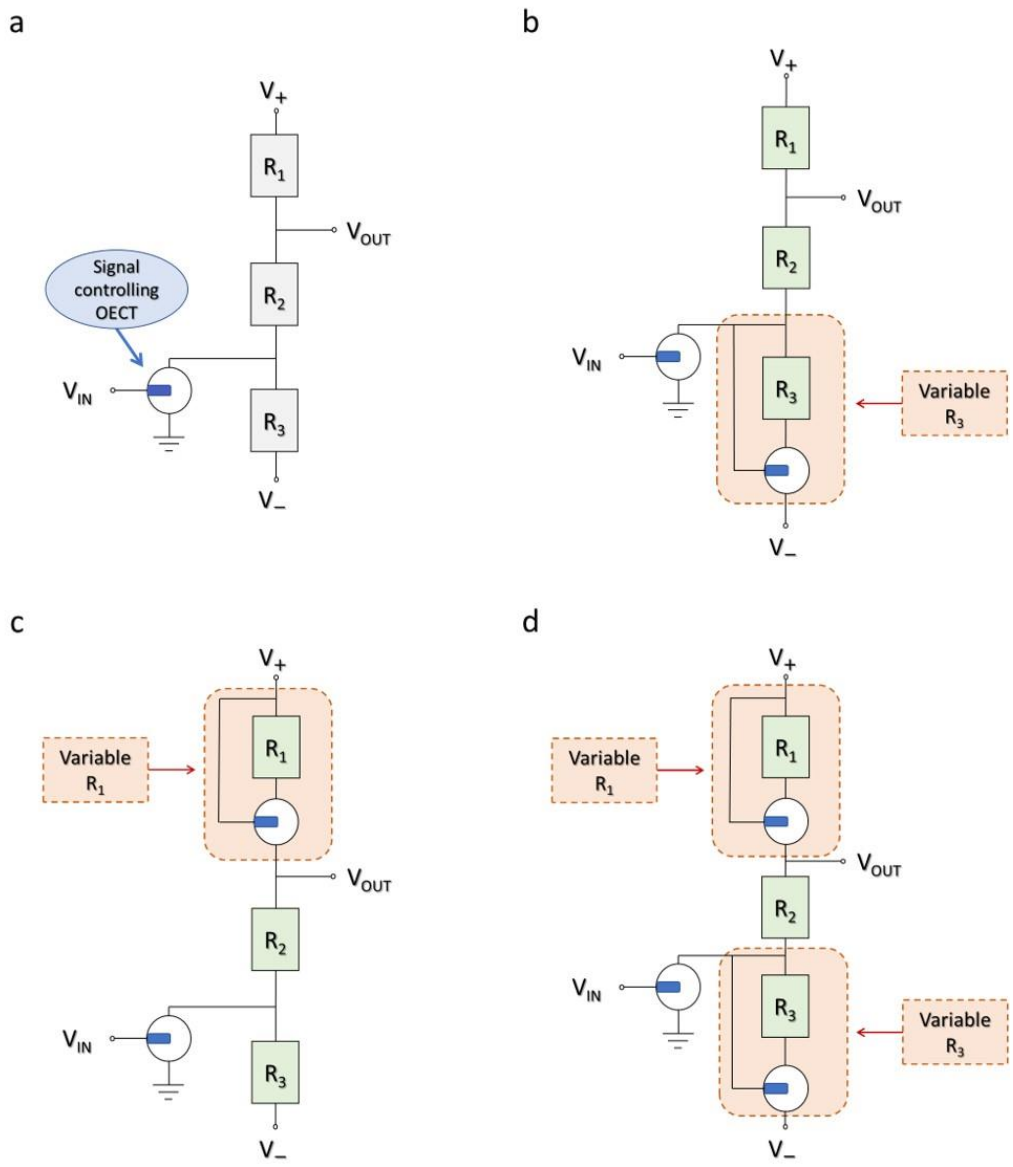

Figure 2: OECT-based inverter designs: (a) 1T design[19] (b) 2T-R_3 design, (c) 2T-R_1 design and (d) 3T design.

As reported recently[19], the 1T inverter (R_1 = 57.6 kΩ, R_2 = 19 kΩ and R_3 = 41 kΩ) with a supply voltage set of +4.43/-4.42 V delivers output levels which coincide with those of the input signal. However, here, by using the same resistor ladder while lowering the supply voltages to +/-2.5 V, the inverter performance declines, as shown in **Figure S2**. This indicates that the combination of low supply voltages (+/-2.5 V) and using the same resistor ladder deteriorates the performance for the 1T inverter. This is evidenced by a very low voltage gain of 2.3 obtained

from the voltage transfer characteristics (VTC, the plot of V_{OUT} vs. V_{IN} of an inverter) and a small V_{OUT} window (cf. Figure S2). It is noted that the advantage of this inverter design is that it leads to relatively faster devices due to having only one OECT in the structure.

2.3 2T-R_3 inverter

The 2T-R_3 design (cf. Figure 2b) is most similar to the 1T inverter (cf. Figure 2a), the only difference is the variable R_3 in the 2T-R_3 inverter structure. Therefore, R_1 and R_2 can be identical with the resistors chosen for the 1T inverter. An example is shown in **Figure 3**, a measurement focusing on R_1 = 57.6 kΩ, R_2 = 19 kΩ and various R_3: 1, 5, 10, 20, 30 and 41 kΩ, where R_1 and R_2 are identical to the 1T inverter with Low R ladder presented in the recent study[19]. In the 2T-R_3 design, the OECT coupled with R_3 works as a variable resistor as the gate voltage (V_G) of the coupled OECT varies during the switching of the inverters. For instance, based on simulations using the SPICE model[16], the block of an OECT coupled with R_3 (1 kΩ) gives a variable resistance between 2.1 and 4.0 kΩ due to that V_G varies between 0.19 to 0.51 V upon switching the inverter at a supply voltage set of +/-2.5 V.

In this design, low R_3 values lead to a higher voltage gain peak, while the voltage gain approaches 0 for R_3 values exceeding 20 kΩ. Figure 3a presents the dependency of the voltage gain peak, $V_{OUT,H}$ and $V_{OUT,L}$ for different R_3 values in breadboarded 2T-R_3 inverters for +/-2.5 V voltage supply, while **Figure S3** shows the results for +/-2 V voltage supply.

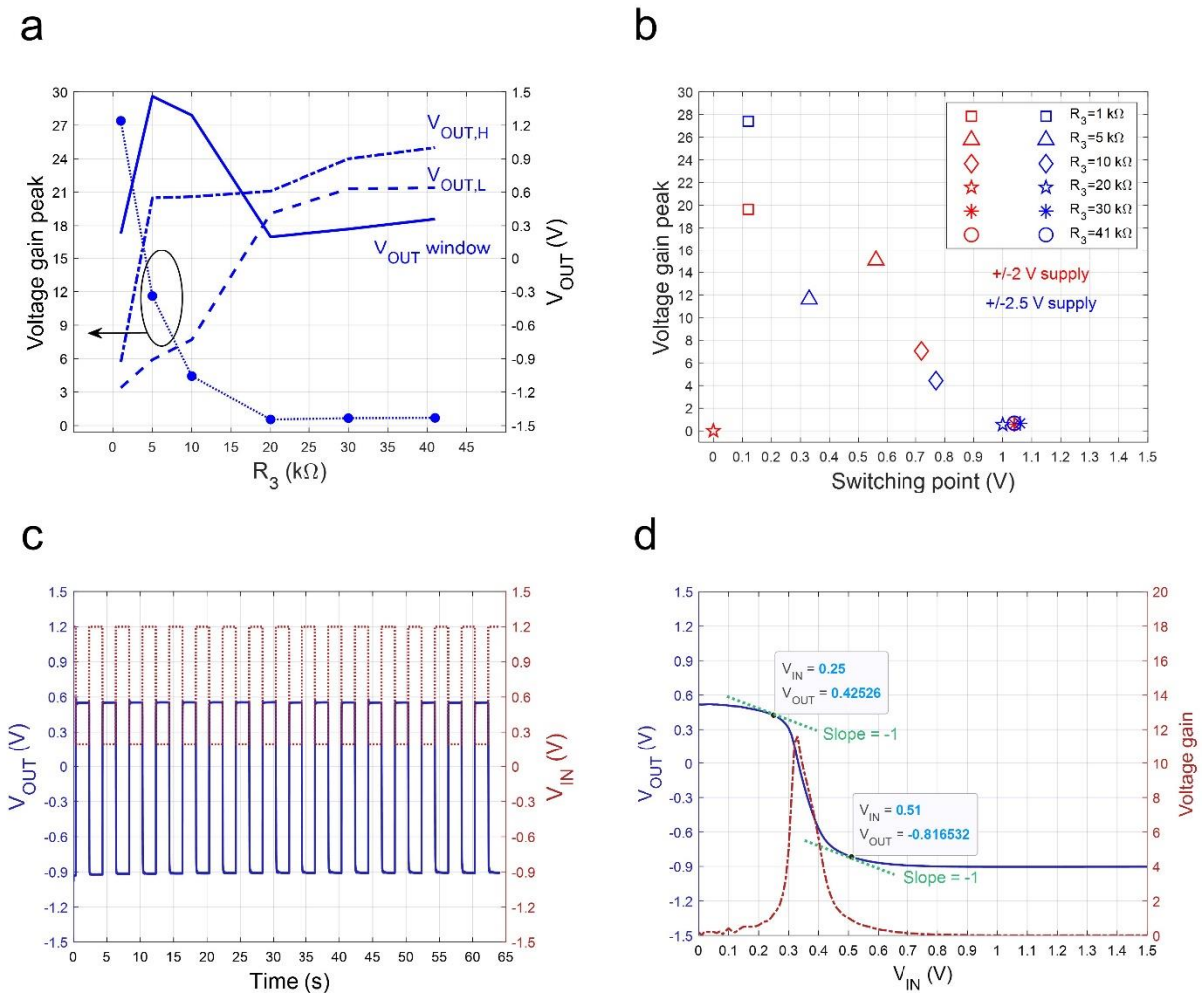

Figure 3: Breadboarded 2T-R_3 inverter based on R_1 = 57.6 kΩ and R_2 = 19 kΩ. (a) The effect of R_3 on voltage gain and V_{OUT} levels while operating the inverter with +/-2.5 V supply voltage and stepping R_3 (R_3 = 1, 5, 10, 20, 30 and 41 kΩ). (b) The effect of R_3 on voltage gain and the relationship between R_3 and the switching point. (c) The switching behavior of the inverter at 0.25 Hz using V_{IN} = [0.2/1.2] V with +/-2.5 V supply voltage and R_1 = 57.6 kΩ, R_2 = 19 kΩ and R_3 = 5 kΩ, and (d) the voltage transfer characteristics of an inverter using the same supply voltage and resistor values where the dotted green lines show the tangent points at which the slope of the VTC curve is equal to -1.

As Figure 3a shows, the V_{OUT} window has a peak at the R_3 resistance values of 5 kΩ and 10 kΩ. Furthermore, this graph shows that the voltage gain peak depends strongly on R_3. In VTC (Figure 3d), the voltage gain peak is observed at a certain V_{IN} value, establishing a well-defined switching point. Furthermore, there is a parameter closely related to the inverter's VTC that is

called noise margin (NM). Inverters can endure levels of noise in both low and high states without compromising the logic operation. These NM levels are stated with NM_L for the low and NM_H for the high noise margins. In the low state the noise margin is given by $NM_L = |V_{IN,L} - V_{OUT,L}|$ while in the high state it is defined as $NM_H = |V_{OUT,H} - V_{IN,H}|$ where $V_{IN,L}$, $V_{IN,H}$, $V_{OUT,L}$ and $V_{OUT,H}$ values are extracted from the inverter's VTC points at which the slope is -1. In Figure 3d the tangent lines with slope of -1 are shown with green dotted lines. The NM_L and NM_H values of 1.06 and 0.09 V are respectively achieved for the 2T-R_3 inverter. Presenting the overall NM as a percentage given by $(NM_L+NM_H)/V_+$ results in a relatively large NM of 46% for this inverter design. Figure 3b presents the switching points associated with each R_3 value for two different sets of supply voltages. According to Figure 3b, by increasing R_3 the switching point shifts towards higher voltages. This means that with higher R_3 a higher V_{IN} is required for a full switching. Looking at Figure 3a, we see that by selecting a too low or too high value for R_3, the V_{OUT} window and/or voltage gain peak are negatively affected. For instance, although the lowest R_3 value (1 kΩ) leads to the highest voltage gain peak, it results in too low V_{OUT} levels that are located at negative voltages. It is noted that the V_{OUT} levels and voltage gain peak exhibit a similar trend for both sets of voltage supplies (Figure 3a and Figure S3). As shown in Figure 3b, for R_3 = 20 kΩ when applying +/-2 V, the voltage gain is zero (indicated with a red star) due to a flat curve obtained in the inverter transfer sweep. This implies that this inverter is not functioning for this specific combination of resistances and supply voltages. For R_3 = 20 (at +/-2 V supply voltage), 30 and 41 kΩ (for both sets of supply voltages), small (non-zero) voltage gain peak values are observed at V_{IN} around 1 V, which is due to the trivial voltage transfer behavior shown in Figure 1. That is, inverters based on these three large R_3 operate with inadequate switching. Figure 3c and d exemplify the dynamic switching measurement and the VTC, respectively, for the 2T-R_3 inverter with the best performance according to Fig 3a (supply voltage of +/-2.5 V and R_1 = 57.6 kΩ, R_2 = 19 kΩ and R_3 = 5 kΩ). The simulation results of the switching performance of the inverter at 0.25 Hz using V_{IN} = [0.2/1.2] V with +/-2.5 V supply

voltage and R_1 = 57.6 kΩ, R_2 = 19 kΩ and R_3 = 5 kΩ can be found in **Figure S4**. The simulated results of the switching behavior are in good agreement with the experimental results (cf. Figure 3c and Figure S4c). Based on Figure 3c, the rise (10% V_{OUT} - 90% V_{OUT}) and fall (90% V_{OUT} - 10% V_{OUT}) transition times of 32 ms and 70 ms are extracted, respectively. Based on Figure S2a, the rise (10% V_{OUT} - 90% V_{OUT}) and fall (90% V_{OUT} - 10% V_{OUT}) times for the 1T inverter are 970 ms and 28 ms, respectively, while the V_{OUT} window is small and decreases even further over time. According to Figure 3, a very important aspect of 2T inverters is that they offer the possibility to control the V_{OUT} levels, voltage gain and switching point by selecting the R3 value, which is not feasible in the 1T inverter. Hence, this design provides significant improvement in the inverter performance as compared to the 1T inverter at low supply voltages (+/-2.5 V). It should be mentioned that the negative part of the V_{OUT} window could be tuned by changing to a non-symmetric voltage supply.

A fully integrated 2T-R_3 inverter has been implemented as shown in **Figure 4a** to demonstrate the possibility of making fully printed versions of such inverters. The measured values of the resistor ladder are R_1 = 20 kΩ, R_2 = 22 kΩ, R_3 = 2.5 kΩ due to variations in the printing process. Dynamic switching with V_{IN} = [0.2/1.2]V at two sets of supply voltages is shown in Fig 4b. Using +/-3 V as the supply voltages, the achieved $V_{OUT,H}$ and $V_{OUT,L}$ are 1.45 V and 0.5 V (V_{OUT} window of 0.95 V), respectively. By adjusting the supply voltage to +2.5 V/-3.5 V, the screen printed inverter delivered $V_{OUT,H}$ and $V_{OUT,L}$ at 1.2 V and 0.15 V, respectively, which is a 5% increase in the obtained V_{OUT} window and a relatively large window as compared to the 1T inverter operated at lower supply voltages (**Table 1**).

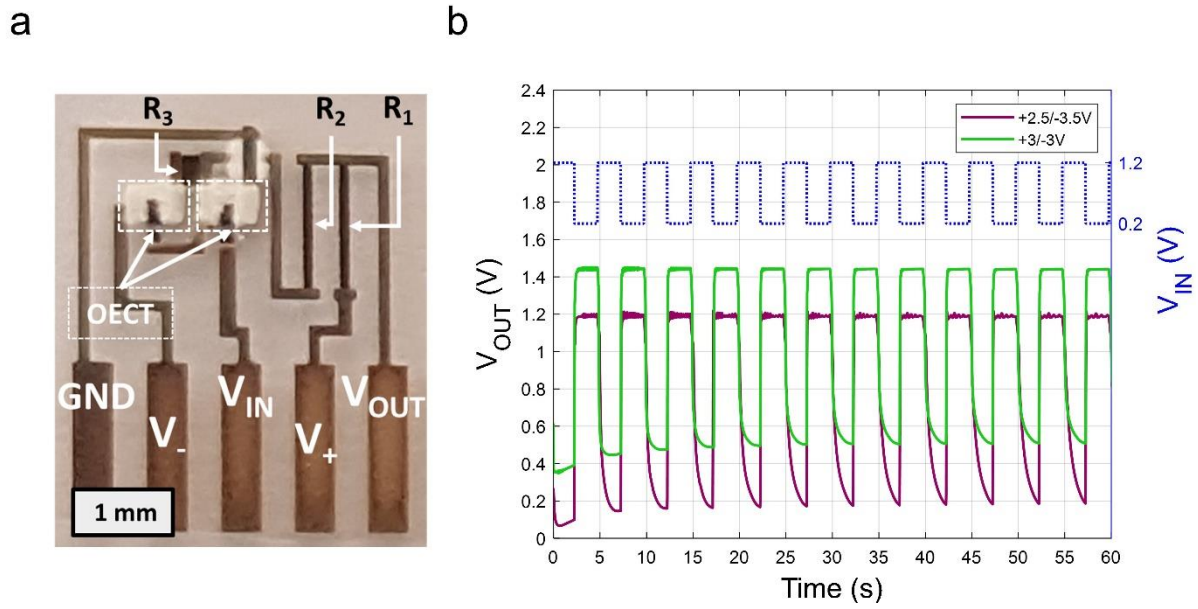

Figure 4: Fully screen printed 2T-R_3 inverter. (a) A microscope image of the printed 2T-R_3 design, (b) the switching behavior of the inverter at 0.2 Hz with R_1 = 20 kΩ, R_2 = 22 kΩ, R_3 = 2.5 kΩ resistor ladder and V_{IN} = [0.2/1.2]V by using +2.5/-3.5 V and +/-3 V supply voltage sets.

As Figure 4b shows, by applying V_{IN} = [0.2/1.2]V, a V_{OUT} window of 1 V is obtained. Due to the lower resistances in the printed resistors, compared to the design, the output voltage is shifted to [0.45, 1.45] V with +/-3 V voltage supply. To counter this effect, an asymmetric voltage supply of +2.5/-3.5 V can bring the output voltage to the desired window [0.15 1.2] V. It is also noted that a V_{OUT} window larger than 1 V can be achieved either by applying larger supply voltages or a higher $V_{IN,H}$ level.

2.4 2T-R_1 inverter

In this inverter design (cf. Figure 2c), the load OECT coupled with R_1 works as a variable resistor where the total resistance should be the largest among the three resistors in the ladder. **Figure S5** shows simulations results, with the SPICE model[16], providing information about the

relationship between different R_1 and R_3 values and the corresponding V_{OUT} levels. This is useful to guide the selection of optimal resistor values for the 2T-R1 design. According to the simulated V_{OUT} levels in Figure S5a, when the resistance of R_1 varies from 5 kΩ to 100 kΩ, the V_{OUT} window gradually increases and saturates at ~1.4 V. However, with increasing R_1 the whole V_{OUT} window shifts towards negative values and $V_{OUT,H}$ decreases below 1 V, which is not sufficient for the next logic stage. Thus, to achieve a large V_{OUT} window and desired logic voltages, the R_1 should be within 35 to 40 kΩ. The resistance of R_3 decides the switching voltage in the VTC of 2T inverters. In general, a smaller R_3 means switching at lower V_{IN}, and this is observed in the measurements presented for 2T-R_3 in Figure 3b. As Figure S5b shows, when the resistance of R_3 increases from 5 kΩ to 100 kΩ, the V_{OUT} window shrinks and $V_{OUT,L}$ increases significantly. For the 2T-R_1 design, the targeted R_3 should be within 15 to 25 kΩ. Compared to the 2T-R_3 design, the relatively large R_1 in the variable resistor block makes the load OECT operate in the subthreshold region which is close to the OFF state of the OECT. The V_G of the load OECT in the variable R1 block varies between 0.96 to 1.1 V (simulated results with the SPICE model) when the inverter switches at a supply voltage of +/-2.5 V and R_1 = 35 kΩ, then R_2 = 60 kΩ and R_3 = 25 kΩ are subsequently selected.

To experimentally evaluate this design, the resistor ladder of R_1 = 35 kΩ, R_2 = 60 kΩ, R_3 = 25 kΩ is explored together with its derivatives to evaluate the tolerance of resistance shifting that sometimes occurs in the screen printing process. Here, a resistor derivative is referred to either the half or one third of the original value of a resistor. That is, one of the resistors in the inverter resistor ladder is modified to half or one third of its original value, while the other two resistors in the ladder are maintained.

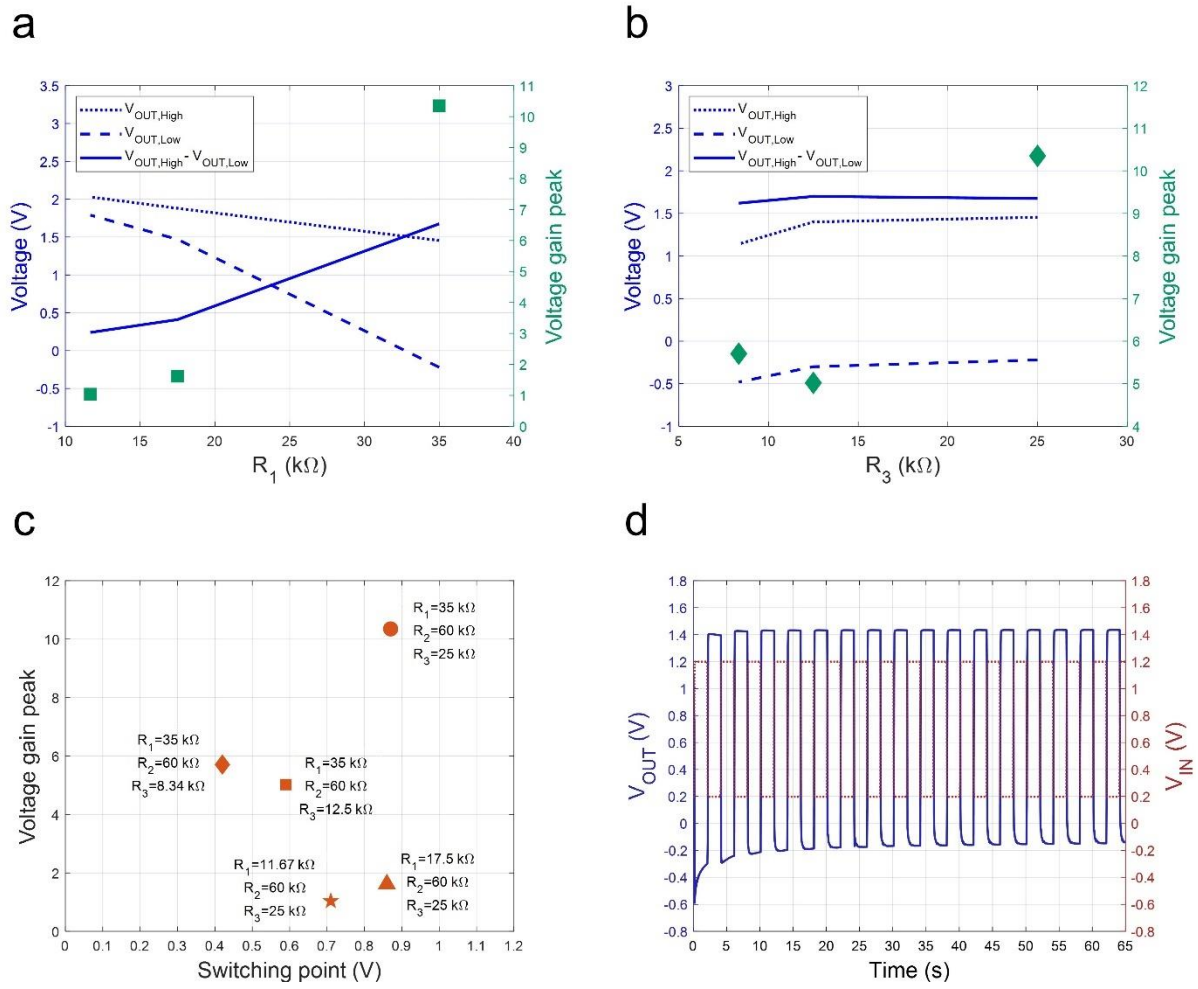

Figure 5: Breadboarded 2T-R_1 inverter performance with +/-2.5 V supply voltage. (a) The dependency between the V_{OUT} levels and the voltage gain peak for different R_1 with fixed R_2 = 60 kΩ and R_3 = 25 kΩ, (b) the effect on voltage gain peak and V_{OUT} levels upon varying R_3 while using R_1 = 35 kΩ and R_2 = 60 kΩ, (c) the relationship between voltage gain peaks and switching points when using the R_1 = 35 kΩ, R_2 = 60 kΩ, R_3 = 25 kΩ resistor ladder and its derivatives, and (d) dynamic switching with V_{IN} = [0.2/1.2]V at 0.25 Hz when using the R_1 = 35 kΩ, R_2 = 60 kΩ, R_3 = 25 kΩ resistor ladder.

In **Figure 5a** the dependency between the V_{OUT} levels and the voltage gain peaks for different R_1 with fixed R_2 = 60 kΩ and R_3 = 25 kΩ is shown, while Figure 5b presents the effects on the voltage gain peaks and the V_{OUT} levels for various R_3 when using R_1 = 35 kΩ and R_2 = 60 kΩ.

Larger R_1 values shifts $V_{OUT,L}$ more rapidly towards lower values, as compared to $V_{OUT,H}$, which implies an enlarged V_{OUT} window. By fixing R_1 = 35 kΩ and R_2 = 60 kΩ, and instead changing R_3 from 8.34 kΩ to 25 kΩ, results in minor increment of the V_{OUT} window while the voltage gain peak is almost doubled, as illustrated in Figure 5b. Figure 5c presents the relationship between voltage gain peaks and switching points when using the R_1 = 35 kΩ, R_2 = 60 kΩ, R_3 = 25 kΩ resistor ladder and its derivatives. As shown in Figure 5c, by keeping R_2 and R_3 fixed at 60 kΩ and 25 kΩ, respectively, while increasing R_1 from 11.67 kΩ to 35 kΩ, an increment in the voltage gain peak is observed. Also, by lowering R_1 = 35 kΩ and R_3 = 60 kΩ to half and one third of their original values, the switching points vary and the voltage gain maximum values are declined. Moreover, by lowering R_1 = 35 kΩ to 17.5 kΩ and 11.67 kΩ shifts the voltage gain peak positions towards lower switching points. Besides, by lowering R_3 = 25 kΩ to half and one third of its original value, the voltage gain values are reduced. Furthermore, as shown in Figure 5c, by increasing R_3 from 8.34 kΩ to 25 kΩ, the switching point shifts towards higher voltages. Hence, higher R_3 implies the requirement of higher V_{IN} to enable full switching. For this inverter design when R_1 = 35 kΩ, R_2 = 60 kΩ, R_3 = 25 kΩ are employed, the NM_L and NM_H values of 0.97 and 0.17 V are obtained, respectively. The overall NM gives a relatively large percentage of 45% for this inverter design.

Figure S6 illustrates experimental results of the voltage transfer sweep and the corresponding voltage gain of the 2T-R_1 inverter using +/-2.5 V supply voltage and R_1 = 35 kΩ, R_2 = 60 kΩ and R_3 = 25 kΩ in the resistor ladder. In Figure 5d, the V_{OUT} signal is monitored with respect to time when the inverter with the resistor ladder R_1 = 35 kΩ, R_2 = 60 kΩ, R_3 = 25 kΩ is switching with a square wave V_{IN} signal alternating between 0.2 V and 1.2 V at 0.25 Hz. From Figure 5d, the rise (10% V_{OUT} - 90% V_{OUT}) and fall (90% V_{OUT} - 10% V_{OUT}) times of 80 ms and 300 ms are extracted, respectively. Although the low level of the V_{OUT} signal is situated at negative voltage amplitudes, the obtained V_{OUT} window is almost 67% larger than the 1 V

window applied as the V_{IN}. This indicates that by having a V_{IN} window of 1V, it is feasible to obtain a V_{OUT} window of 1.67 V. The simulated results of the switching behavior shown in Figure S4a are in good agreement with the experimental results (cf. Figure 5d). The results are also further approved by simulating the 3-stage ring oscillator based on the 2T-R_1 inverter design when employing the resistor ladder R_1 = 35 kΩ, R_2 = 60 kΩ and R_3 = 25 kΩ (cf. Figure S4b). By using R_1 = 35 kΩ, R_2 = 60 kΩ, R_3 = 25 kΩ as the resistor ladder, the voltage gain maximum occurs at 10.35, while assembling the inverter with the derivatives of this resistor ladder pulls the voltage gain peak down, as indicated by Equation (6). The V_{OUT} levels obtained from the VTC (cf. Figure S6) are in good agreement with those observed in the dynamic switching (cf. Figure 5d) measurement. The resistances in the ladder affect the inverter switching behavior in terms of expected V_{OUT} window and other parameters. Hence, such observation is expected from the simulations presented in Figure S5.

In brief, Figure 5 again proves the potential of the inverter designs for achieving tunable and high voltage gain as well as large V_{OUT} windows. Moreover, this inverter design shows further improvement compared to the 2T-R_3 inverter performance in terms of higher V_{OUT} window. That is, the V_{OUT} window of 1.46 V for the 2T-R_3 (with the R_1 = 57.6 kΩ, R_2 = 19 kΩ, R_3 = 5 kΩ resistor ladder) increased to 1.67 V for the 2T-R_1 with the resistor ladder R_1 = 35 kΩ, R_2 = 60 kΩ, R_3 = 25 kΩ. However, the voltage gain peak values, in the range of ~10-11, achieved for these two designs are almost similar.

Similar to the 2T-R_3 inverter, a fully-integrated 2T-R_1 inverter has also been implemented by screen printing. A microscope image of this 2T-R_1 inverter is shown in **Figure 6a** with the actual resistor ladder measured to R_1 = 18 kΩ, R_2 = 38 kΩ and R_3 = 25 kΩ.

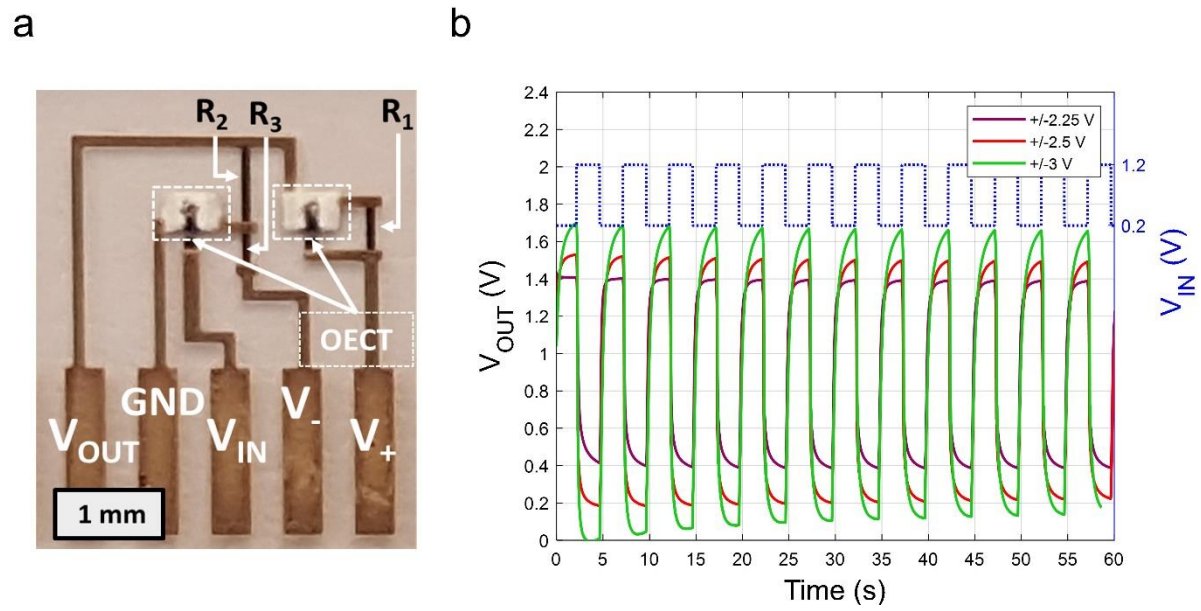

Figure 6: Fully screen printed 2T-R1 inverter. (a) Microscope image of a printed 2T-R1 design and (b) the switching behavior of the inverter at 0.2 Hz with V_{IN} = [0.2/1.2]V and a resistor ladder of R_1 = 18 kΩ, R_2 = 38 kΩ, R_3 = 25 kΩ while using three supply voltage sets of +/-2.25 V, +/-2.5 V and +/-3 V.

The dynamic switching curves in Figure 6b show that a 1 V input window [0.2/1.2 V] and the supply voltages of +/-3 V will result in a large V_{OUT} window with 1.7 V and 0.1 V as V_{OUT} levels, and even when the supply is lowered to +/-2.25 V, the V_{OUT} window is still 1 V (with V_{OUT} levels of 1.4 V and 0.4 V).

2.5 3T inverter

The 3T inverter can be viewed as a combination of the 2T-R_3 and 2T-R_1 inverter layouts. As such, it will benefit from two variable resistors in the ladder. Therefore, the R_1 for this design is selected to the value tested for the 2T-R_1 inverter with R_1 = 35 kΩ. Similarly, based on the 2T-R_3 inverter, the R_3 value is chosen for this design. Thereby, the load OECTs are designed with the resistors R_1 = 30 kΩ and R_3 = 2 kΩ, while R_2 = 31 kΩ is subsequently selected to

deliver the desired $V_{OUT,L}$ and $V_{OUT,H}$. When the inverter switches with the supply voltages of +/-2.5 V, for the load OECT coupled with R_1, a V_G range between 1.05 to 1.1 V is expected, while the load OECT coupled with R_3 experiences a V_G ranging between 0.7 and 0.14 V, as provided by simulation results using the SPICE model.

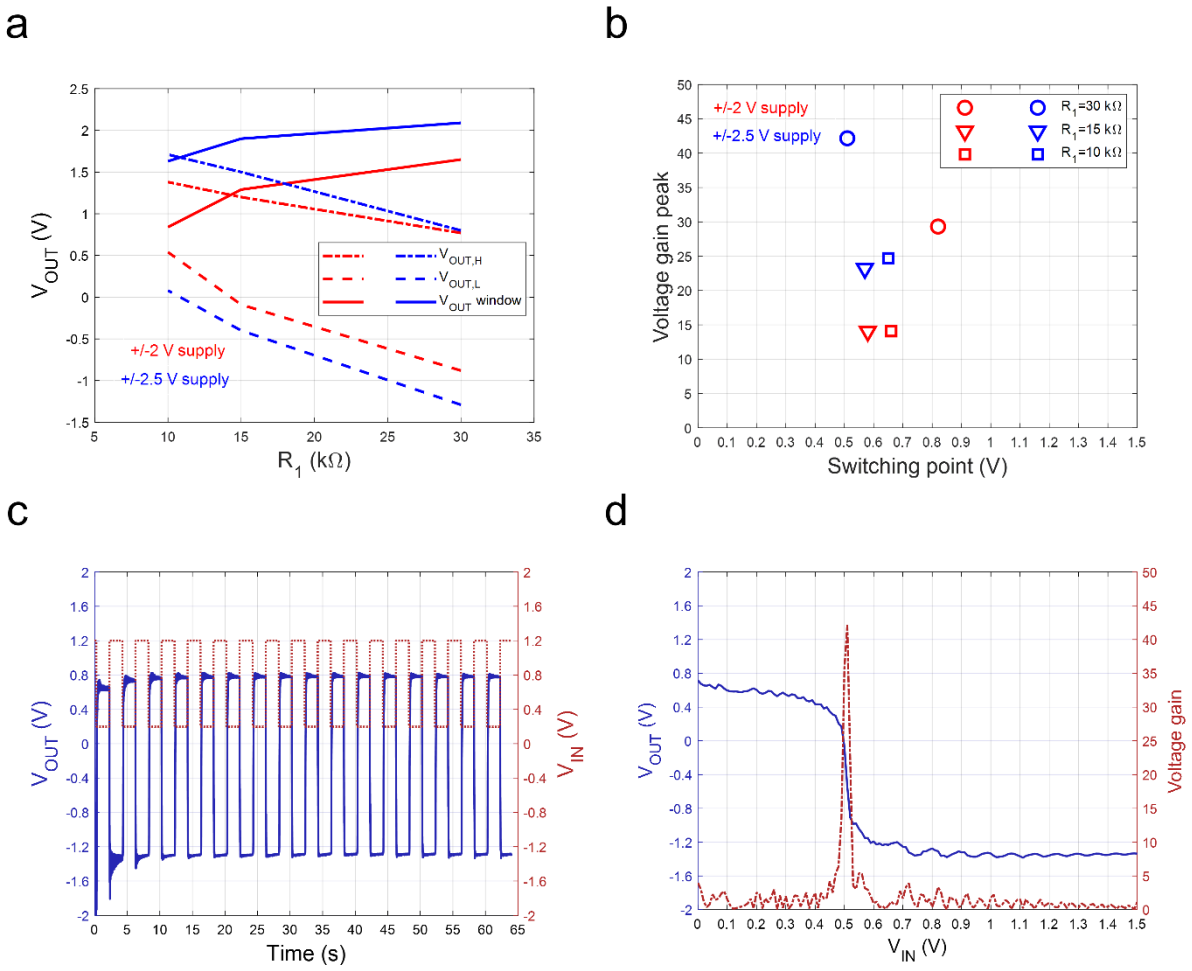

Figure 7: Breadboarded 3T inverter performance. (a) Relationship between V_{OUT} levels and different R_1 with fixed R_2 = 31 kΩ and R_3 = 2 kΩ operating with +/-2 V and +/-2.5 V supply voltages, (b) the effect of different R_1 on the voltage gain peak and switching point while using fixed R_2 = 31 kΩ and R_3 = 2 kΩ, (c) dynamic switching behavior of the inverter with R_1 = 30 kΩ, R_2 = 31 kΩ and R_3 = 2 kΩ and a V_{IN} signal switching between 0.2 V and 1.2 V at 0.25 Hz, (d) transfer sweep of an inverter based on the R_1 = 30 kΩ, R_2 = 31 kΩ and R_3 = 2 kΩ resistor ladder.

Figure 7a shows the effect of varying R_1 on the V_{OUT} levels obtained from the experiment while keeping R_2 and R_3 fixed to 31 kΩ and 2 kΩ, respectively. By increasing R_1, both $V_{OUT,H}$ and $V_{OUT,L}$ levels move towards more negative values with a faster change for the $V_{OUT,L}$, thereby causing the V_{OUT} window to expand. As shown in Figure 7b, reducing R_1 from 30 kΩ extensively decreases the voltage gain peak value. Since R_3 is fixed, the switching point does not shift significantly when R_1 varies between 10 kΩ to 30 kΩ. We also note that the highest voltage gain (42) of all investigated inverter configurations in this report is measured for the 3T inverter with the resistor ladder R_1 = 30 kΩ, R_2 = 31 kΩ and R_3 = 2 kΩ. The dynamic switching behavior of the inverter with the same resistor ladder is shown in Figure 7c for input levels varying between 0.2 V and 1.2 V at 0.25 Hz and supply voltages of +/-2.5V. The simulated results of the switching behavior are in good agreement with the experimental results (cf. Figure 7c and Figure S4d). Based on Figure 7c, the rise (10% V_{OUT} - 90% V_{OUT}) and fall (90% V_{OUT} - 10% V_{OUT}) transition times of 130 ms and 100 ms are extracted, respectively. Based on Figure 7c, $V_{OUT,H}$ and $V_{OUT,L}$ levels of ~0.8 V and ~-1.3 V are obtained, yielding a large output window of 2.1 V. The corresponding inverter transfer sweep is presented in Figure 7d, where the V_{OUT} levels are in good agreement with those observed from dynamic switching (cf. Figure 7c). It is worth mentioning that for the 3T inverter with the resistor ladder R_1 = 30 kΩ, R_2 = 31 kΩ and R_3 = 2 kΩ, the NM_L and NM_H values of 1.58 and 0.10 V are obtained, respectively. This means that for this inverter design, the overall NM gives the percentage of 67%, which is largest among the inverter designs presented in this work.

As exemplified by the voltage amplification and V_{OUT} window, the 3T inverter design shows higher performance than both the 2T-R_1 and 2T-R_3 inverter designs.

Comparing designs

The V_{OUT} window, voltage gain and switching point are the three important parameters of the inverter performance. To obtain an inverter with optimal performance, a good trade-off between these three factors is of great importance. For instance, an inverter with high voltage gain but small V_{OUT} window is not practically useful in any circuit. Table 1 presents the best performing inverters from each design operating at supply voltages of +/-2.5 V and V_{IN} levels alternating between 0.2 V and 1.2 V at 0.25 Hz. It is noted that the overall NM values, expressed as a percentage, are given by $(NM_L+NM_H)/V_+$, i.e., at half of the supply voltage.

Table 1: Summary of the best performing breadboarded inverters, the data are recorded from each design operating at +/2.5 V supply voltage, 0.25 Hz and [0.2/1.2] V as the input signal.

Inverter design	Resistors (kΩ)	Voltage gain peak	Noise margin	Switching point (V)	$V_{OUT,L}$ (V)	$V_{OUT,H}$ (V)	V_{OUT} window (V)
1T	R_1 = 57.6 R_2 = 19 R_3 = 41	2.30	17%	0.46	0.04	0.53—0.26	0.49—0.22
2T-R_3	R_1 = 57.6 R_2 = 19 R_3 = 5	11.61	46%	0.33	-0.91	0.55	1.46
2T-R_1	R_1 = 35 R_2 = 60 R_3 = 25	10.35	45%	0.87	-0.22	1.45	1.67
3T	R_1 = 30 R_2 = 31 R_3 = 2	42.17	67%	0.51	-1.29	0.8	2.09

As Table 1 states, the 1T inverter (standard OECT-based inverter) gives the lowest voltage gain and the smallest V_{OUT} window among all inverter designs. However, by using higher supply voltages, e.g., +4.43/-4.42 V[19], coincided input and output voltage levels can be attained. By shifting from the 1T to the 2T-R_3 inverter design, the voltage gain and V_{OUT} window is increased by 8.5 times and 3 times, respectively. By altering the inverter design from 2T-R_3 to 2T-R_1, the voltage gain drops by ~11% while the V_{OUT} window increases from 1.46 V to 1.65 V. The 3T inverter, which is the combination of the 2T-R_3 and 2T-R_1 designs, gives the best performance in terms of both voltage gain and V_{OUT} window. Thus, by going from the 1T inverter to the 3T inverter, we achieve an improvement of the voltage gain and V_{OUT} window values by more than 18 times and almost 6 times, respectively. Based on Table 1, the switching points for the 1T, 2T-R_3 and 3T inverters have approximately similar values, while for the 2T-R_1 inverter this value occurs at 0.7 V, which the highest value among all designs. Again, it is noted that the negative part of the V_{OUT} window could be tuned by changing to non-symmetric supply voltages. The noise margin values presented in Table 1 are based on $(NM_L+NM_H)/V_+$ for each inverter design. The highest noise margin was obtained for the 3T inverter design, while the 1T inverter design resulted in the lowest value. This means that by shifting from the 1T to the 3T inverter design, the noise margin is improved by 50%, and a logic circuit based on the 3T inverter design is more robust.

In brief, based on the VTC of the inverters, both voltage gain and noise margin can be evaluated. From a voltage gain standpoint, the output voltage transition occurs between the $V_{OUT,L}$ and $V_{OUT,H}$ levels. A steep voltage transition leads to a high voltage gain peak. Also, when the plateau of the $V_{OUT,H}$ level is reached at a reasonably low V_{IN} level, the voltage gain peak occurs at a relatively low switching point. From a noise margin perspective, the slope of VTC is equal to -1 at two coordinates defined by [$V_{IN,L}$, $V_{OUT,H}$] and [$V_{IN,H}$, $V_{OUT,L}$]. A small difference between the $V_{IN,L}$ and $V_{IN,H}$ levels results in a steep voltage transition and hence a high voltage

gain peak. Since NM_L is defined as $|V_{IN,L} - V_{OUT,L}|$, a small $V_{OUT,L}$ is desired to obtain a large NM_L. As NM_H is described as $|V_{OUT,H} - V_{IN,H}|$, a large $V_{OUT,H}$ is required to achieve a large NM_H.

Figure 8 compares this work versus previously reported logic inverters relying on printed PEDOT:PSS-based OECTs[5,15,18,19] in terms of voltage gain peak values and the corresponding switching points.

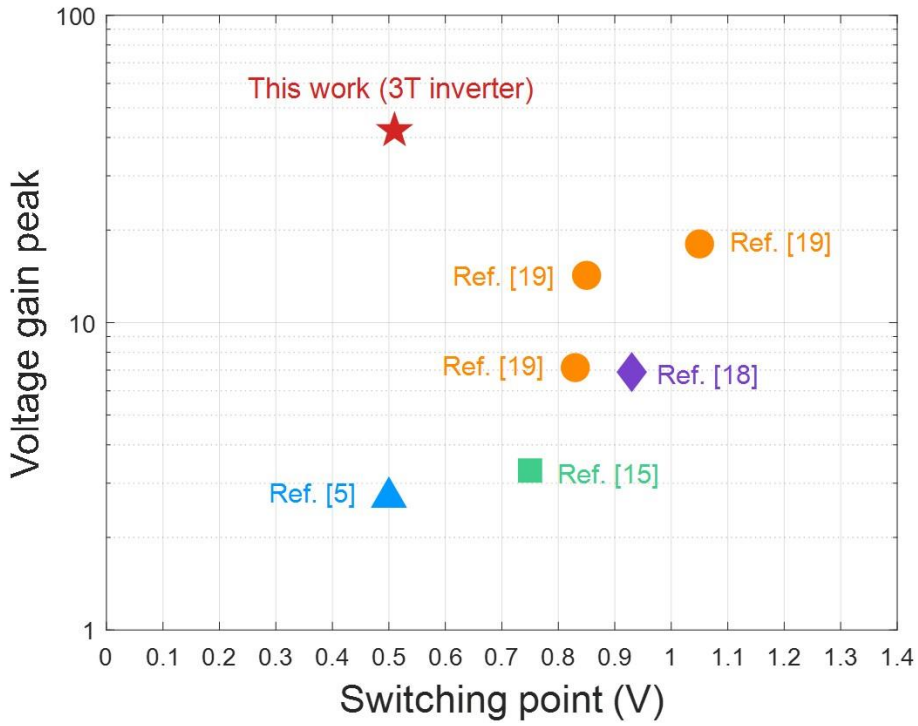

Figure 8: Benchmark of inverters relying on printed PEDOT:PSS-based OECTs[5,15,18,19] in terms of voltage gain peak values and switching points (the V_{IN} value at which the voltage gain peak is observed).

The voltage gain achieved here with the 3T inverter design is, as far as we are concerned, the highest reported value for inverters based on printed PEDOT:PSS OECTs[5,15,18,19].

3. Conclusions

Novel screen printed OECT-based inverter structures with channel dimensions of 150×100 μm^2 were designed and explored, aiming to improve their overall performance. The new inverter designs originate from standard OECT-based inverters, in which variable resistances in the structures were achieved by either coupling an additional OECT with one of the resistors in the resistor ladder, or by coupling two additional OECTs with two of the resistors. The performance of the inverters was investigated in terms of voltage gain, noise margin, V_{OUT} levels and switching point.

In the 2T-R_3 inverter design, which is the design most similar to the standard 1T inverter, the additional OECT was coupled to R_3, thereby creating a variable R_3 in the inverter structure. This results in a voltage gain that is ~5 times higher as compared to the 1T inverter, and a tunable switching point range of approximately 0.5-1.0 V. The noise margin achieved for this design 30% higher than that of the 1T inverter.

The 2T-R_1 design is created by coupling an additional OECT with R_1 to create a variable R_1 in the inverter structure. Here, the voltage gain exceeds 10, which corresponds to an increase by a factor of ~4.5 as compared to the 1T inverter. The determining factor for the voltage gain value is the resistor ladder, as also predicted by simulations. A V_{OUT} window of 1.67 V is obtained for a 1 V peak-to-peak input signal. The noise margin attained for this inverter design was close to that of the 2T-R_3 design.

The 3T inverter design, with two additional OECTs in the structure, was realized by combining the 2T-R_3 and the 2T-R_1 designs. A resistor ladder with R_1 = 30 kΩ, R_2 = 31 kΩ, R_3 = 2 kΩ, plus some variations thereof, were experimentally evaluated. A voltage gain of 42 and a switching point of 0.51 V were achieved. This is the highest voltage gain value accomplished

for printed inverters relying on standard PEDOT:PSS-based OECTs with resistor values limited to only tens of kΩ in the resistor ladder. This inverter design showed the highest noise margin, which can result in circuits with a high range of tolerance for the logic voltage levels. This was expected since this inverter showed the highest voltage gain value.

There is a trade-off between the selected resistor values, the voltage gain, noise margin and the V_{OUT} window. The switching point varies for different inverter designs, and it also depends on the selected resistor values in the ladder. Our proposed OECT-based inverter designs offer tunable voltage gain and V_{OUT} levels, which paves the way for electronic circuits where the power supply is limited and high voltage gain is essential.

4. Experimental Section

4.1 OECT and inverter fabrication

The layout of OECTs and inverters are created by using Clewin software (*WieWeb Software Inc., Netherlands*). Based on the design layout, the devices are manufactured by the following screen printing process. On a polyethylene terephthalate (PET) plastic substrate the following eight layers are screen printed on top of each other. First, silver (*Ag 5000 purchased from DuPont*) ink is printed to create probing lines. Then a layer of PEDOT:PSS (*Clevios S V4 purchased from Heraeus*) is printed as the channel material. Afterwards, a carbon (*7102 conducting screen printing paste purchased from DuPont*) paste is printed as the source and drain electrodes in the third layer. These three layers are cured by thermal means. The next step is to print an insulating (*5018 purchased from DuPont*) layer, followed by UV curing. The area defined by the insulating layer is then covered by an electrolyte ink (*E003 provided by RISE*) in the next printing step. Another PEDOT:PSS layer, serving as the OECT gate electrodes, is printed on top of the electrolyte as the sixth layer, to finalize the OECT structures. For the

printed inverters, a resistive carbon (*7082 purchased from DuPont*) paste is printed to create the resistor ladder. Finally, yet another silver layer is printed to create line crossings.

4.2 Characterization and measurements

The printed devices were stored and measured at a temperature of ~20° C and a relative humidity of ~50 %RH. The inverters were either fully screen printed or assembled on a breadboard by using screen printed OECTs and passive resistors. For the characterization of OECTs and inverters, a semiconductor parameter analyzer (*HP/Agilent 4155B*) and a function generator (*Agilent 33120 A*) were used.

Acknowledgement

This project has received funding from the Swedish foundation for Strategic Research (Silicon-Organic Hybrid Autarkic Systems, Reference number: SE13-0045), the Knut and Alice Wallenberg Foundation (Wallenberg Wood Science Center and Wallenberg Scholars), and the European Union´s Horizon 2020 research and innovation programme under the grant agreement Nos 825339 (WEARPLEX) and 964677 (MITICS). MB gratefully acknowledges support from the Önnesjö Foundation.

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